REMARKS

[0014] Submission: This Submission responds to the FOA dated June 24, 2004, and accompanies the enclosed Request for Continued Prosecution.

[0015] Summary: By this Submission, the specification has been amended to correct typographical errors and to consistently refer to nouns. Claims 4, 5, 14-20, and 24-28 have been canceled without prejudice to the patentability of the subject matter of the canceled claims. The remaining claims have been amended to clarify certain features, and claim 30 has been added. In response to the rejections based on art, arguments are made for the patentability of the pending claims.

[0016] Amendments To The Specification: Entry of the amendments to the Specification is respectfully requested. To correct typographical and grammatical errors, amendments are made to pages 1, 5, 6, 8, 11, 14, and 16. The amendments to the paragraph starting at page 4, line 3 correct the nouns for reference numbers 208 and 210. The amendments to the paragraph starting at page 4, line 9 correct the noun for reference number 208, and correct the grammar in re "devices". The amendments to the paragraph starting at page 6, line 17 correct the name of the controller consistently with that at page 14, line 5. The amendments to the paragraph starting at page 10, line 21 conform the name of the buses to the reference numbers. The amendments to the paragraph starting at page 11, line 20 conform the use of "bus segments" to the previous discussion of bus segments. The amendments to the paragraph starting at page 13, line 16 conform the use of "bus segments" to the previous discussion of bus segments, and correct the reference number 304 to conform to Fig. 3. The amendments to the paragraph starting at page 17, line 3 conform the name of the bus segments to the reference numbers, and corrects the

grammar in re the resetting and bus segment isolation operations. These amendments are informal in nature, and no new matter has been added. Thus, entry of these amendments to the Specification is believed to be in order, and is respectfully requested.

[0017] Amendments To The Claims: Entry of the amendments to the claims is respectfully requested. The amended claims are based on the disclosure of the drawings and specification. For example, the amendment to the preamble of claim 1 is shown in Fig. 3, wherein the first bus segment is 310, the expander is 304, and the coupling is only to the second bus segment 312. Paragraph b) is amended to clarify that the "in response" clause applies to the two resetting operations (expander and devices) and the "establishing...reset isolation mode" operation. This conforms to the description of the reset signal at page 11, lines 13-15 (expander and device reset), and at page 14, lines 5 to line 19 (first expander isolates the reset signal). The modes are described at page 14, line 10 (reset isolation) and segment isolation mode at page 16, line 18, for example. Paragraph c1) is amended consistent with the description at page 16, line 18 in re segment isolation mode, and at page 11, lines 10-19 in re reset signal resulting in the claimed expander isolating all signals (line 18). The reference to busy signal is supported at page 16, lines 17 through 23.

[0018] Claim 2, 6, 8, 18, 19, and 29 amendments, and new claim 30, relate to how reset is performed one bus segment at a time. This is supported at page 9, lines 4-7, page 12, lines 4-6, page 17, lines 12-15, and at page 18, lines 8-17. The amendments also conform to Fig. 3, which shows the bus segment 314 as a third bus segment, and the host computer 302 connected only to the first bus segment 330, hence configured to assert the reset signal only on the first bus segment. The reset being prevented from propagating to the third bus segment follows from the

description at page 11, lines 16-17. The reset signal resulting in the claimed expander isolating all signals is supported at page 11, line 18. The claim 8 amendment to "...the first expander exits the segment isolation mode..." etc. is supported by the above descriptions at pages 9, 12, 17, 18 in re "...expander exits...reset one bus segment at a time by repeating the above process, proceeding...to the most distant bus segment...", and at page 14, lines 5-11 in re reset isolation mode. The claim 18, 19, and 29 amendments, and claim 30, are based on the above descriptions in re claims 2, 6, and 8.

[0019] Claim 7 amendments conform to the first and second bus segments now defined in respective claims 1 and 9.

[0020] Claim 9 amendments conform to Fig. 3, which shows the bus segment 314 as a third bus segment, and the host computer 302 connected only to the first bus segment 330, hence configured to assert the reset signal only on the first bus segment. The amendments conform further to Fig. 4 which shows the expander coupled to prevent the reset signal from propagating through the expander controller 402, where the reset signal is received by the expander controller from the first bus segment through the first I/O interface circuit and to the first reset and segment isolator controller. The "during the period" text clarifies the temporal aspects of signal isolation by defining a time period, which occurs after the isolating of the reset signal and until the bus in the first bus is cleared.

[0021] Claim 11 and 13 amendments conform to page 17, lines 23-24 onto page 18, lines 1-3.

[0022] Claim 21 amendments conform to Fig. 4 which shows the controller 408 coupled between only the first and second I/O circuits. The modes are described at page 14, line 10 (reset isolation) and segment isolation at page 15, lines 9-12 and page

16, line 18, for example. The page 14, line 10 discussion shows that the reset isolation mode is entered in response to the RST_A reset signal, which is applied on the first bus segment whether or not the second bus segment is in a not hung condition. Fig. 4 and the page 14 discussion supports the clause relating to the reset signal received by the expander controller from the first bus segment through the first I/O interface circuit and to the first reset and segment isolator controller.

[0023] Claim 23 amendments clarify the temporal aspects of reset signal isolation by defining when the second bus is hung in relation to isolation of the reset signal and being in or out of the segment isolation mode, which conforms to the description at page 17, lines 3-9, for example.

[0024] It is respectfully submitted that the claim amendments are either to correct informalities, or are supported by the Specification. Thus, entry of the amendments to the claims is believed to be in order, and is respectfully requested.

[0025] Response To Assertion That Arguments Against References Individually Cannot Show Nonobviousness When Rejections Are Based On Combinations of References: Consideration has been given to the Keller and Merck cases cited in the rejection (page 16, lines 3-7, for example). These cases were the basis for objecting to the previous arguments "against the references individually", which were deemed improper due to the nature of the rejections. The rejections are based on combinations of three and four references.

[0026] In response, it is noted that in Merck, the CAFC stated that "non-obviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references." The meaning of this statement was made clear in other remarks of the CAFC that discussed its

holding. Those remarks include a discussion of what is disclosed by the seven references that were combined in the rejection.

[0027] In such discussion, the CAFC not only separately noted what was disclosed in each individual reference, but (see Rey-Bellet, for example) also noted what was not disclosed or taught in that individual reference. See also the review of the Kuhn reference, in which the CAFC noted how it "differs" from the material of another reference. With respect to the one Petersen reference, which was one of the 7 references that were combined, the CAFC read Petersen for what it fairly teaches in combination with the prior art as a whole.

[0028] Review of Merck, for example, clearly shows that in determining "what it fairly teaches in combination with the prior art as a whole", the CAFC:

* separately reviewed each of the 7 references (see "D. The References" in the case),

* in "II. Discussion", separately discussed the Roche Reports, and each of the Friedman, Burger, and Petersen references,

* discussed (see *Prima Facie Obviousness* Section) the combined teaching of the prior art, and

*noted what was not disclosed in a reference and how the reference differed from a material of another reference.

[0029] Similarly, in Keller, the CCPA not only noted what was disclosed in each separate reference, but (see Berkovits, for example) also noted what was not disclosed or taught in that separately discussed reference.

[0030] In view of this analysis of these cited cases, it is respectfully submitted that the following remarks are set forth consistently with the approach of the CAFC in the Merck and Keller cases. For example, these remarks properly separately review

each of the four references here cited, including what is disclosed and not disclosed, and properly discuss the combined teachings of the prior art (see paragraphs [0090] + in re *Prima Facie* Obviousness). Further, these remarks properly identify what teachings of essential principles of operation must be changed to result in a combination of references having claim limitations. Also, these remarks properly identify those claim limitations that are not contained in the combined teachings. It is respectfully requested that the objection not be repeated with respect to the following remarks

[0031] Review of Claimed Invention: Each amended claim defines at least a first bus segment and a second bus segment, with an expander between only those two bus segments. Each bus segment still includes a set of devices and a bus that is coupled to the set of devices. In response to a reset signal asserted on the first bus segment, operations of claims 1-3, and 6-8, and 30 reset a first expander that is coupled to the first bus segment. Also in response, a first reset isolation mode is established so the first expander isolates that reset signal, which is not propagated to the second bus segment. After those resets, a segment isolation mode prevents communication signals from propagating between the first and second bus segments so that a busy signal from the second bus will not propagate to the first bus segment and thus will not interrupt the clearing of the first bus segment. The reset isolation mode continues, and if the bus of the second bus segment is hung, a far-side reset signal resets the bus of the second bus segment, and the expander in the reset isolation mode prevents this far-side reset signal from being propagated to the first bus segment. If the bus of the second bus segment is not hung, the far-side reset is not needed because the reset of the first bus segment cleared the bus hang situation. Exiting from both the segment isolation mode and the reset isolation mode allow propagation of signals between the

first and second bus segments.

[0032] The reset isolation mode always prevents the reset signal on the first bus segment from propagating to any other bus segment. Only the first bus segment is cleared in response to that reset signal. Any new reset signal (far-side) is applied only to the next (e.g., second) bus segment (i.e., not to the third bus segment), and only in response to that next (second) bus segment being hung-up. Each claim defines the basic resetting of only one bus segment at a time, i.e., defines at least reset of the first bus segment and then (if necessary) reset of the second bus segment, and (if necessary) reset of the third bus segment. This sequential operation is more efficient than concurrent resetting, because the first bus segment starts operations as soon as it is reset, and the resetting of any next subsequent bus segments is isolated from the now-operating first bus segment, for example. Also, if the next bus segment is found to be not hung-up, the inter-bus segment operations start immediately.

[0033] All claims define either operations or structure for isolation of the reset signal (applied to the first bus segment) from the second bus segment, and resetting of an expander and devices of one bus segment, all achieved one bus segment at a time starting with the first bus segment and going to the second bus segment. Further, a third bus segment is defined in amended claims 2, 6, 8, 18, 19, and 29, and in new claim 30. This bus segment-by-bus segment reset limitation is defined by:

(1) a particular reset isolation controller of an expander controller (amended claims 9 and 21) is connected between <u>only</u> the first and second I/O circuits;

(2) such reset isolation controller (amended claims 9 and 21) is adapted to isolate the reset signal received on the <u>first</u> bus segment, so that the reset signal does <u>not</u> propagate <u>through the expander</u> controller to the <u>second</u> bus segment

(amended claim 9), and to prevent the reset signal from propagating to the second bus segment whether or not the second bus segment is in a not bus hung condition (amended claim 21);

(3) the first bus segment is coupled by an expander only to the second bus segment (amended claims 1, 9, and 21), which results in what is described in this paper as a "series connection" of the first bus segment and the second bus segment through the expander, and through the I/O interfaces (claim 21); and

(4) in response to the reset signal asserted on the first bus segment (amended claim 1), the expander coupled between only the first bus segment and the second bus segment operates in a reset isolation mode to isolate the reset signal asserted on the first bus segment such that the reset signal is not propagated through the first expander to the second bus segment.

[0034] By these multiple and sequential operations, and by the elements of amended independent claims 9 and 21 that isolate the reset signal from the second bus segment, the functioning of the second bus segment is not interfered with by the reset signal that would otherwise be applied from the first bus segment to each particular expander that may be connected to one such second bus segment. The segment isolation mode of the expander allows the reset first bus segment to clear. That segment isolation occurs temporally, that is, during the period after the reset signal is isolated and until the bus in the first bus segment is cleared from a hang condition. Further, by the reset isolation mode, the far-side reset signal is not communicated back to the now-cleared first bus segment. The now-cleared first bus segment therefore operates independently of the resetting of the later bus segments.

[0035] Discussion of Each of The References Separately As A Preface To Showing the Combined Teaching of All Three or Four Cited References: These discussions are set forth below as follows:

House: Paragraphs [0036] +, Looi paragraphs [0041] +,

Ehata paragraphs [0050] +, and IBM paragraphs [0075] +.

[0036] First Discussion: House:

[0037] Background: House In Rejections In FOA: The rejections of claims 1-8 relate House only to the elements set forth in the preamble of claim 1, for example. Thus, House shows a first bus 26 with devices 22; a second bus 28 with devices 24; and an extender 30 between buses 26 and 28. House does not provide reset signals and operation in response to reset signals for clearing bus hang. Oppositely, House waits for buses to self-clear, in that House teaches (col. 11, lines 51+) that the extender 30

> "monitors the BUSY... line to detect termination of ... data transfer, which would result in a bus free phase and permit another SELECTION..."

The lack of reset signals and lack of operation in response to reset signals for clearing bus hang is consistent with page 5 of the FOA (top of page), where the FOA admits that House does not expressly teach the first two of the claimed steps of the six steps claimed. Thus, as to claim 1, House does not teach an operation of asserting a first reset signal on the first bus segment, nor of resetting a first expander in response to the first reset signal on the first bus segment. Further, House does not show the first expander responding to any such reset signal to establish a reset isolation mode to isolate such reset signal from being propagated through the first expander to the second bus segment. By reference to the FOA discussion in the rejection of House

taken with Looi and Ehata (page 4, lines 5+), it is apparent that House also does not teach the claimed operation of isolating all communication signals between the first and second bus segments.

[0038] Disclosure In House: Applicants Submit That The Following Is The Proper House Disclosure: It is respectfully submitted that one skilled in the art would reasonably interpret House in the manner described in paragraphs [0038] through [0040] below. House shows a first bus 26 with devices 22; a second bus 28 with devices 24; and an extender 30 between buses 26 and 28. House also shows the transceivers 42 and 44 as I/O interface circuits connected to the respective first and second bus segments 26 and 28, and those transceivers 42 and 44 are connected to an expander controller 46, 48, and 50 between the I/O circuits. As noted, however, in describing the operation of the expander controller, House teaches that the extender 30

> "monitors the BUSY... line to detect termination of ... data transfer, which would result in a bus free phase and permit another SELECTION..." (col. 11, lines 51+), and
>
> "the extender waits until the main bus becomes free and then arbitrates for control. During this time, the auxiliary bus 28 is hung, and no communication on that bus takes place." (col. 12, lines 8-11).

[0039] Essential Principle Of Operation: The House teaching of waiting until the main bus becomes free, indicates that House teaches of an essential principle of operation, which is that no overt action should be taken to interfere with busy operation of the hung second bus segment 28 and devices 24. This essential principle of operation indicates first, that that House does not teach the claimed reset and isolation controller of the claimed expander controller, because the resetting of the claimed operation and structure do interfere with the operations of the hung second

bus segment. Further, the admissions at FOA page 7, lines 5-7 and at page 9, lines 15-18, are consistent with the above indication of the teaching of such wait, etc., and are consistent with the fact that House does not teach the claimed reset and isolation controller of the claimed expander controller, and does not teach a reset signal, and does not teach the expander controller for isolating a reset signal, as claimed.

[0040] It is submitted that there is no disclosure in House that would suggest to one skilled in the art, or that would motivate, one skilled in the art to combine House with any of the features of the other three references. This is confirmed, for example, by the rationales in the FOA at pages 3, lines 11-15, and at page 7, lines 15-20, and at page 10, lines 3-8. In each case, no reference is made to House as suggesting or motivating combination. Further, the rebuttal remarks in the FOA at page 17, lines 1-2, for example, do not identify a suggestion or motivation based on House.

[0041] <u>Second Discussion: Looi</u>: (applied to claims 1-8 and claims 10, 13, 16, 18, 22, 25, 27, and 29)

[0042] <u>Background: Looi In Rejections In FOA:</u> The FOA asserted (FOA pages 17, lines 22-24, and page 17, lines 1-5), that Looi's method relates to the Looi embodiment of Fig. 1 (see page 17, line 23). In re Looi Fig. 1, in the FOA a first bus segment was said to be expansion bus 61, a second bus segment was said to be expansion bus 62 (FOA page 18, line 3), and the expander was said to be bridge 60 (FOA page 17, line 19). The reset signal (FOA page 3, line 5) was said to be the local bus reset signal (the number of which was not cited). At FOA page 13, lines 22-24, it was said that the Looi "bus expander bridge 50 of Fig. 1" resets expander bridge 60 in response to an (unnumbered) "reset signal", and a cite was made to col. 6, lines 26-31. Further, at FOA page 14, lines 16-18 and 19-23, it was asserted that Looi's SCSI expander controller (e.g., bus expander bridge 50 of Fig. 1) enters into a reset

isolation mode (i.e., reset state) in response to said reset signal (See col. 6, lines 26-31). Thus, a reset isolation mode of bridge 50 was said to be a "reset state". Still further, at FOA page 15, lines 5-8 it was asserted that in Looi a first bus segment is expansion bus 61 in Fig. 1, and that Looi asserts a reset signal "on said first bus segment", citing "(See col. 4, lines 12-16 and 42-44)". Thus, it was asserted that bus 61 is a first bus segment. Further, at FOA page 15, lines 17-19, it was asserted that in Looi bus segments 51 and 61 are reset one segment at a time from a first bus segment (i.e., Expansion bus 61 in Fig. 1; see col. 1, lines 6-10 and col. 6, lines 12-63). Thus, it was asserted that Looi's bus segments 51 and 61 in Fig. 1 are reset one segment at a time from the first bus segment 61.

[0043] Disclosure In Looi Based On FOA: Operation of Bridge 60: The following remarks show that, in the context of the presently-claimed invention, Looi is not properly interpreted as having the claimed first and second bus segments be those shown as 61 and 62. The FOA asserted (FOA pages 17, lines 22-24, and page 17, lines 1-5, and FOA page 15, lines 5-8) that in Looi a first bus segment is expansion bus 61 in Fig. 1, and that Looi asserts a reset signal "on said first bus segment". The page 15 assertion cited "(See col. 4, lines 12-16 and 42-44)". In response, reference to Looi at the cited col. 4 indicates that at lines 12-16 the response of bridge 50 to reset signal is described. Such response is that bridge 50 outputs reset signals 58 and 59 on respective buses 51 and 52. In the context of the claims, it is bus 45 (re bridge 50) or bus 46 (re bridge 60) that is part of a "first" bus segment, such that bus 61 would not be part of a first bus segment. Taking bridge 60 as an example applicable also to bridge 50, it is acknowledged that in Looi Fig. 1 the bridge 60 is connected to each of the bus 61 and 62. However, the bridge 60 is also connected to a further bus 46 to receive and respond to a reset control signal 64.

Thus, the bus 61 is not coupled by the expander 60 only to the asserted second bus segment 62, as now claimed. As to the asserted reset signal (the "local bus reset signals 68 and 69"), two such local bus reset signals are taught, i.e., signal 68 on bus 61 and signal 69 on bus 62 (col. 4, lines 29-33). Those local signals are applied to buses 61 and 62 by the expander bridge 60. The operation of the expander bridge 60, for example, is in response to the different (not cited) reset control signal 64 applied to the bridge 60 by controller 40 (col. 4 , line 20). That operation of bridge 60 in response to the reset control signal 64 is (col. 4, line 21) to reset the bridge 60, and to output both of those asserted local bus reset signals 68 and 69 to respective buses 61 and 62 (col. 4, lines 29-33). Thus, contrary to the assertion, the bridge 60 does not respond to the asserted local bus reset signal 68 that is on the asserted "first" bus segment 61. Further, the response of bridge 60 to signal 64 shows that the bridge 50 does not reset bridge 60 as asserted in the FOA. Col. 6, lines 26-31 do not teach that bridge 50 provides signal 64 to the bridge 60. Rather, the cited Looi col. 6, lines 26-31 relates to a timing diagram of Fig. 3. The description at col. 6, lines 12-35 includes signal flow from controller 40, which is coupled to both bridges 50 and 60 which are to be selected for use in expansion from the controller 40. At col. 4, lines 20-23, the description makes it clear that bridge (expander) 60 is not reset in response to the local bus reset signal 68. Rather, bridge (expander) 60 is reset in response to the reset control signal 64 from controller 40. Col. 6, line 22 says

> "asserting the reset control signal coupled to the bus expander bridge identified by the received command..."

This "identified" is how the selection of the bridge 50 or 60 occurs. For example, in response to the signal 64 the bridge 60 is selected. Consistent with the signal 64

identifying selection of bridge 60, Fig. 1 and col. 4, lines 25-27 show the reset control signal as 64, and teach

> "...when bus control signal 64 is asserted by master bus controller 40 to reset bus expander bridge 60, ..."

which is an example of resetting bridge 60, which resetting is not in response to a signal on the asserted "first" bus segment 61. Also, there is no operation of bridge 60 in response to the local bus reset signal 68. Further, the bridge (expander) 60 is not caused to isolate the local bus reset signal 68 from the asserted second bus segment (as claimed), because the bridge 60 in fact applies both of the local bus reset signals 68 and 69 to the respective buses 61 and 62, which is in effect a transmission through the bridge 60 of the initial reset signal 64. Therefore, Looi is not properly interpreted as having the claimed first bus segment be that shown as 61, nor as having that bridge 60 (or 50) perform a reset signal isolating function.

[0044] Applicants' Comments: Reset State of Looi Bridge 50: The following remarks show that neither bridge 50 nor 60 enters into a reset isolation mode, as claimed. In paragraph [0042] above, it was noted that the FOA asserted (page 14, lines 16-23) that the Looi bus expander (bridge 50 of Fig. 1) enters into a reset isolation mode, and in the FOA this was equated to a "reset state". Such mode was said to be in response to "said reset signal". In response, referring to the cited col. 6, lines 26-31, the timing diagram of Fig. 3 is described. At col. 6, lines 26-31, an example is given in which it is the bridge 60 that is "identified", such that bridge 60 has been "selected" for the expansion, and bridge 50 is idle (i.e., not doing an expansion). Col. 6, lines 26-27 clearly state that the "reset 1 control 540" to bridge 50 "remains in a de-asserted state", which means that there is no reset signal 54 applied to the bridge 50 in this example of Fig. 3. Rather, in response to reset signal

64, bus 46 to bridge 60 is in a reset state at 461, and as shown at lines 31-34, reset signals 680 and 690 are asserted at 691 and 681, corresponding to the output local bus reset signals 69 and 68, respectively, described at col. 4, lines 25-29. Assuming that the rejection meant to refer to the active (expanding) bridge, here bridge 60, it is respectfully submitted that the active bridge 60 has no reset isolation mode. Referring to the combination of disclosures of Figure 3 and col. 4 and col. 6, these teach that in this example: (1) bridge 50 is not isolating a reset because it is idle, and (2) the active expander (bridge 60) is also <u>not isolating</u> the reset signal 64 because the response to the reset signal 64 is to output two <u>reset</u> signals 68 and 69. As a result, neither bridge 50 nor 60 enters into a reset <u>isolation</u> mode. Consistent with this teaching of no reset isolation mode, the description of Looi below (paragraph [0046]) does not attribute any such reset isolation mode to Looi. It is further respectfully requested that in any further Office Action assertion of Looi, the referenced assertion at FOA page 14, lines 15-23 not be repeated.

[0045] <u>Applicants' Comments: Resetting Bus Segments One At A Time:</u> Further, as to FOA page 15, lines 17-19, it was asserted that Looi's bus segments 51 and 61 in Fig. 1 are reset one segment at a time from the first bus segment 61 (see end of paragraph [0042] above). The above remarks in paragraph [0043] show that the bus 61 is not part of a "first" bus segment in the context of the claimed invention. Rather, in Looi, the resetting of successive bus segments occurs in response to the reset (selection) signals from controller 40. A separate reset signal 54 is applied to bridge 50. Because bridge 50 and its buses and devices are separate from bridge 60 and its buses and devices, when the bridge 50 reset operation has been completed, another separate signal (64) is applied by the controller 40 (not by the bridge 50) to bridge 60. The claims have been clarified and

set forth (independent claim 1) coupling of the first bus segment only to the second bus segment, and the reset operation initiated in response to only one reset signal asserted on that first bus segment. Similarly, independent claims 9 and 21 provide that the I/O interface circuits are coupled only to respective first or second bus segments, for example.

[0046] Disclosure Of Looi Based On Proper Interpretation of Looi: It is respectfully submitted that one skilled in the art would reasonably interpret Looi in the following, different manner, a manner which is more consistent with House, and with claims 1-8 (subject to the exceptions noted below), and which is also based on Fig. 1. In this manner of interpretation, the bus 46 is part of a first bus segment. The second bus segment includes the bus 62, also asserted by the rejection as a second bus segment (FOA page 18, line 3). This is consistent with the House showing of its first bus segment connected to one "side" of an expander 30 and a second bus segment connected to an opposite "side" of that same expander 30. In a House + Looi combination, the reset control signal 64 is the claimed reset signal applied to the first bus segment 46 and to which the bridge 60 (expander) responds, and which House lacks. A third bus segment would include the bus 61, with appropriate devices. The reset control signal 64 causes the bridge (expander) 60 to be reset (col. 4, lines 22-23). However, as one exception noted above, in response to this reset control signal 64, the bridge 60 outputs the two local bus reset signals 68 and 69, one to each of buses 61 and 62 of respective second and third bus segments. The bridge 60 thus simultaneously outputs a reset signal to each of two parallel second and third bus segments (including the respective buses 61 and 62) such that all devices coupled to each of the two separate bus segments are reset by the respective local bus reset signal 68 or 69. Such output of reset signals 68 and 69 is through the expander (bridge) 60

and is in response to the original reset control signal 64, such that the reset signal 64 is effectively not isolated from each of the two (second or third) bus segments of which buses 61 and 62 are part.

It is further respectfully submitted that this interpretation of Looi in this paragraph [0046] is not a "voluntary interpretation" of Looi simply for purposes of argument (as was asserted at FOA page 17, line 21 in re Applicants' comments in re Looi Fig. 2). Rather, such interpretation is based on the very same Fig. 1 of Looi that was asserted in the FOA, and is consistent with that Fig. 1 of Looi (columns 3 and 4 of Looi describe Fig. 1). Moreover, that FOA rejection could not properly assert that the bridge (expander) 60 of Looi responds to the local bus reset signal 68 (on asserted first bus 61) because Looi teaches that the bridge 60 itself applies that signal 69 to the bus 62 (in response to the reset signal 64). Moreover, in response to the reset signal 64, the local reset signals 68 and 69 are output on the second and third bus segments without regard to the state (hung or not-hung) of the buses 61 and 62.

[0047] Looi Teaching of Essential Principle of Operation: No Isolation Of Reset Signal: It is respectfully submitted that the simultaneous output of the two local bus reset signals 68 and 69, one to each of buses 61 and 62, is a teaching of an essential principle of operation of Looi. That teaching is that:

> the reset control signal 64 must be applied to the bridge 60, and when the reset control signal 64 is applied to the bridge 60, the bridge (expander) 60 should not isolate the original reset control signal 64 from either of the above-described (paragraph [0046]) second or the third bus segments (that include the buses 61 and 62), and that such reset signal 64 should appear on the two buses 61 and 62 in the form of the respective local bus reset signals 68 and 69 without regard to the state (hung or not-hung) of the buses 61 and 62..

This teaching means that even though the bus and the devices of the second and third buses 61 and 62 are not hung, those buses and the devices of those buses 61 and 62

should and will be reset, and will be reset in response to the reset control signal 64. Further, Looi cannot teach that asserted (FOA page 14, line16-23) reset isolation mode in Looi is in response to the local bus reset signal 68 because that local bus reset signal 68 is applied to the bus 61 by the bridge 60. Further, and oppositely to such assertion, the Looi teaching of connecting the bridge 60 to the bus 46 is part of this essential principle of operation, in that without the bridge 60-to-bus 46 connection, there would not be a response by the bridge 60 to the reset signal 64. If the bus 61 were part of a first bus segment and bus 62 part of a second bus segment, as asserted (FOA page 18, line 3--see paragraph [0042] above), there would be no connection of the bridge 60 to the bus 46, and this essential principle of operation would be changed. Specifically, it would be lost because the reset control signal 64 would not be received by the first bus segment (including bus 61), the bridge 60 would not be selectable, and the local signals 68 and 69 would not be generated. Thus, this essential principle of operation includes the teaching that by the output of local reset signals 68 and 69 the reset signal 64 is not isolated and should not be isolated from second and third buses 61 and 62.

[0048] Looi Teaches Away From Claimed Isolation: Further, it is respectfully submitted that this last-mentioned Looi teaching of an essential principle of operation is a teaching away from the claimed

> **in response to the first reset signal asserted on the first bus segment,** ....establishing a first reset isolation mode of the **first expander** to perform **reset signal isolation** such that the first reset signal is not propagated through the first extender to the second bus segment (amended claim 1);
>
> the first expander controller including a first reset and segment isolation controller coupled between **only the first and second I/O interface circuits** and adapted to **isolate** a reset signal received on the first bus segment so that the reset signal **does not propagate through the second I/O interface circuit**

to the second bus segment, (amended claim 9) ; and

the SCSI expander controller including a reset and segment isolation controller coupled between **only the first and second SCSI I/O** interface circuits and adapted to operate in a reset isolation mode to **isolate a reset signal** received on the first bus segment and **prevent the reset signal from propagating to the second bus segment whether or not the second bus segment is in a not hung condition,** (amended claim 21)

[0049] Looi Teaching of Essential Principle of Operation: No Reset Segment-By- Segment In The Manner Claimed: It is respectfully submitted that another essential principle of operation of Looi is that:

> there must be separate destinations to which the separate reset signals 54 and 64 are transmitted from one controller 40 to obtain the asserted resets "one segment at a time" (FOA page 15, lines 17-19),
>
> wherein the separate destinations operate independently of each other to be reset in response to the respective reset signals 54 and 64.

Those separate destinations are the separate bridges 50 and 60, which are not reset one segment at a time in response to one initial reset signal applied to only one of the bridges (e.g., to only one first bus segment). Further, because this Looi essential principle of operation relies on a second reset signal (54 or 64) from the controller 40 to initiate the next reset of the separate bridge 50 or 60, that next reset is not initiated by a far-side reset from an expander between first and second bus segments, and not on a condition that the next bus segment is hung. It is respectfully submitted that it would require a change in this essential principle of operation of Looi to place a series of expanders between a series of bus segments, and to have a first bus segment receive one and only one reset signal from a host and to propagate further far-side reset signals through the successive expanders to reset each successive bus segment, and to issue the far-side reset signals only if those successive bus segments are hung.

[0050] Third Discussion: Ehata:

[0051] Background: Ehata As Asserted In FOA Rejections: The discussions in the following paragraphs [0052] through [0056] indicate how the various rejections in the FOA characterized Ehata. **Do all relate to isolation??** In one case (see paragraph [0052] below), the rejection did not emphasize Ehata teaching two such bus segments (because House teaches two bus segments). In another case (see paragraph

[0053] below) a rejection asserted that a not hung-up device 2 of Ehata is a first bus segment, and a hung-up device 2 is a second (other) bus segment, and the Ehata circuit 7 acts to isolate a reset signal occurs between those two devices (asserted as two separate bus segments). In another case (see paragraph [0054] below) these rejections asserted that a hung-up device 2 of Ehata is a first bus segment, and a not hung-up device 2 is a second (other) bus segment.

[0052] First FOA Rejections: Pages 19, 20, 21, and pages 12-13: On page 19, lines 19 through 23 (and two lines onto page 20) of the FOA, the rejection asserted that Applicants (1) "misinterpret" the claim rejection, and (2) essentially admits that Ehata does not teach two claimed bus segments. The rejection (page 19, lines 21 and 22) did not assert that Ehata teaches two claimed bus segments. Rather, it indicated, in effect, that it was not necessary for Ehata to teach two such bus segments, because the rejection asserted:

> "House teaches the bus segment of main bus and the bus segment of auxiliary bus correspond to the claimed pair of first and second bus segments, ...".

Further, on page 20, lines 12 through 24, the rejection asserted that Applicants (1) "misinterpret" the claim rejection, and (2) in response to Applicants' argument that Ehata only teaches one of the claimed two bus segments, the rejection again essentially admitted that Ehata does not teach two claimed bus segments. In detail, the rejection (page 20, lines 19 through 22) did not assert that Ehata teaches two claimed bus segments. Rather, it indicated, in effect, that it was not necessary for Ehata to teach two such bus segments, because the rejection asserted:

> "House teaches said two clear bus segments with expander (See the instant Office Action, page 6, line 11 through page 7, line 4), and Ehata suggests the "deficient element", i.e., the claimed subject matter "reset and segment isolation controller".

Further, on page 21, lines 5 through 8 of the FOA, the rejection again did not assert that Ehata shows two bus segments, and only referred to one bus segment:

> "in [sic] contrary to Applicants' argument, Ehata teaches all of the devices of the first bus segment (i.e., all of the hung-up SCSI devices with the SCSI bus) are reset (i.e., clear bus hang) in response to the reset signal (i.e., RST signal)..."

This assertion does not refer to any second bus segments of Ehata, and is consistent with the above two (pages 19 and 20) effective admissions that Ehata does not teach two claimed bus segments. Further, on pages 12 and 13, lines 19 through 23 (onto page 13) of the FOA, the rejection again did not assert that Ehata shows two bus segments, and again referred to House:

> "...to disable propagation of said reset signal (i.e., RST reset signal 6 of Fig. 2; Ehata) to said first and second bus segments (i.e., bus segments of main bus 26 and auxiliary SCSI bus 28 in Fig. 1; House)."

[0053] <u>Second FOA Rejections: Pages 3, 7, and 9</u>: Generally, these rejections assert that a hung-up <u>device</u> 2 of Ehata is a first bus segment, and a not hung-up <u>device</u> 2 is a second (other) bus segment. In detail, the rejections (FOA page 3, line 19; page 7, lines 8-14, and page 9, line 19 to page 10, line 2) asserted that Ehata discloses a reset and segment isolation controller in the form of inverter circuit 7 (e.g., with circuit 71 and OR circuit 72) in Fig. 2. Those circuits 7 (71/72) were said to be adapted to isolate a reset signal (RST signal 6, Fig. 2) received (per col. 2, paragraph [0004]) on a first bus segment (asserted as a hung-up SCSI device in Fig. 1), page 3, line 19, page 7, line 10, and page 9, line 21). The asserted result was said to be that an expander device (SCSI control circuit in Fig. 2) is provided for isolating a reset (RST signal 6) between a pair of bus segments in an I/O subsystem (the SCSI bus system in Fig. 1. Reference was made to col. 2, paragraph [0009] through col. 3, paragraph [0010]). The other (second) bus segment was said to be a not hung-up bus

segment (page 3, line 21 ["other" bus segment is referenced], page 7, line 11; and page 9, line 22). In review, these rejections (1) identify the **devices** 2 of Ehata as "bus segments" (i.e., without any bus), and (2) in effect assert that the circuit 7 of the hung-up device 2 isolates the RST reset signal 6 that is on that hung-up device 2 from a not-hung-up device 2, and that such device-to-device isolation is a bus segment-to-bus-segment isolation. These rejections do not identify the locations of these devices, i.e., do not say where the one hung-up device is or where the not hung-up device is located.

[0054] Third FOA Rejection: FOA Pages 22 and 23: This rejection immediately follows the page 21 rejection and asserts that:

> Page 22, lines 9+:
>
> "in fact, Ehata suggests that the reset RST signal **caused by** the **first** bus segment (i.e., **not hung-up device** and SCSI bus) is isolated...from propagating to the **second** bus segment (i.e., **hung-up** device and SCSI bus). In other words, Ehata describes (1) the **first** bus segment is **not** blocked by the reset-condition judging device for receiving the reset RST signal caused by the first bus segment, (2) the **second** bus segment **is** blocked by the reset-condition judging device for receiving the RST signal caused by the first bus segment at the same time (See paragraph [0007]), which implies that a reset and segment isolation controller isolates a reset signal received on the first bus segment from propagating to the second bus segment"; and

This rejection raises issues as to (1) a first bus segment "causing" an RST reset signal 6, (2) whether a reset-condition judging device of a **not** hung-up bus segment in Ehata would **not** block the RST reset signal 6 "caused by" the first bus segment, and (3) how the RST reset signal 6 **would be blocked** from the not-hung-up second bus segment in Ehata. Again, these rejections do not identify the locations of these devices, i.e., do not say where the one hung-up device is or where the not hung-up device is located.

[0055] <u>Fourth FOA Rejection: Assertion Re: Ehata's Lack of Two Bus Segments:</u> The rejection argued that it doesn't matter that Ehata has only one bus segment. FOA page 19, lines 7-10, and FOA page 20, lines 19-22 asserted that the fact that House teaches two bus segments separated by an expander 30 provides the two claimed bus segments. The House expander 30 was said to lack the claimed reset and segment isolation controller, which is the "deficient element" assertedly provided by Ehata (FOA page 19, line 9, and FOA page 20, line 21). Again, this rejection raises issues as to (1) relationship to the rejections identified in paragraphs [0053] and [0054], (2) how the "deficient element" of House is overcome by the asserted reset and segment isolation controller of Ehata, e.g., where is that controller located?

[0056] <u>Fifth FOA Rejection: FOA Pages 23:</u> This rejection asserts that:

<u>Page 23, lines 9-15 (text expanded for emphasis):</u>

"Instead, Ehata discloses the whole purpose

of not applying that one reset signal to the operating SCSI device

is to allow that having [sic] not hung-up offering [sic] the SCSI control circuit

which avoids reset processing.

Ehata is silent to mention [sic] if the whole purpose of not applying that one reset RST signal to the operating SCSI device is to allow that operating not-hung device to continue operate independently of the hang-up of the other SCSI device on that same bus segment.

Therefore, in contrary [sic] to the Applicants' allegation, Ehata is not teach [sic] away from the limitation "said expander controller isolates all signals to prevent..." in lines 15-17 of the exemplary claims 9, ..."

[0057] Review of Claimed Bus Segments: In defining a bus segment as one device the rejection of paragraph [0054] does not conform to the claimed "first" and "second" bus segments. As claimed, (a) a bus segment is defined a bus and devices, and (b) a first bus segment is the bus segment on which the reset signal is asserted (independent claim 1), or received (independent claims 9 and 21). The reset signal is not claimed as being "caused" by the first bus segment (as is asserted in the FOA page 22 cite). In the claimed isolation this claimed reset signal is asserted or received only on the first bus segment. In amended claims 9 and 21 the controller isolates a reset signal received by the controller from the first bus segment through the first I/O interface circuit. Also, this claimed reset signal would normally propagate to the next (second) bus segment, but because of the isolation it does not so propagate.. Further, only the claimed first bus segment is reset in response to the claimed reset signal received on the first bus segment, and all devices of the first bus segment are reset. As claimed, by the additional far-side reset signal, one thus achieves the reset of one bus segment at a time, which follows from the defined isolation, specific aspects of which are defined in amended claims _2, 6, 8, 18, 19, 29, and 30. Further, the second bus segment is reset by the far-side reset signal only if the second bus segment is hung. To shorten discussion, the claimed bus segments are referred to as being "in series" because, in the absence of the isolation, the claimed reset signal would propagate from the first bus segment to the second bus segment.

[0058] Ehata Devices, As Such, Are Not Claimed Bus Segments: In view of the remarks in paragraph [0056] above, it is clear that the devices 2 of Ehata, as such and without a bus or other devices, are not a "bus segment" as claimed.

[0059] Ehata Teaches One Bus Segment: In Ehata, the RST reset signal 6 is on the one SCSI bus 3. The one SCSI bus 3 with the #1, #2, and #3 devices 2 form the one

bus segment of Ehata. From the one bus 3 the RST reset signal 6 is applied simultaneously to each of the devices 2 that is coupled to the bus 3 on that one bus segment 3. This is also clear from Ehata Fig. 1 in which the bus 3 couples the host 1 to three devices 2 of the one bus segment. As noted in paragraph [0055] above, the rejection argued that it doesn't matter that Ehata has only one bus segment.

[0060] The RST Reset Signal 6 Is Not Applied From One Device To A Next Device Or Other Bus Segment: The justification for ignoring the failure of Ehata to teach two bus segments, was that House shows two claimed bus segments. According to the rejection noted in paragraph [0055] above, Ehata provides the isolation device missing from House, which is asserted as the circuit 7 described in paragraph [0053] above. However, Ehata teaches that the circuit 7 is in each of the devices 2 on the one Ehata bus segment. None of those devices 2 and none of those circuits 7 in those devices 2 is interconnected to another device so that after an RST reset signal is applied to one device 2 that RST signal 6 can be applied to any other device 2. Thus, in contrast to the above (paragraph [0056]) reference to the claimed two bus segments being "in series" (such that a reset signal could be transmitted from one claimed bus segment to a next claimed bus segment as in House, see amended claim 1), in Ehata Fig. 1 there is no "series connection" of the devices 2. Instead, the Ehata disclosure is that once an RST signal 6 is received on any one Ehata device 2, such RST signal 6 either (a) appears on and resets the SCSI controller 4 of that same one device, or (b) that RST signal does not appear on the SCSI controller 4 of the one device 2. In the absence of the circuit 7 the reset signal would not exit the device 2. Ehata thus does not assert the RST reset signal on only the first bus segment in a manner by which the first reset signal is normally transmitted through the circuit 7 to some second bus segment (amended claim 1), for example.

[0061] The RST Signal Is Not "Caused By" The First Bus Segment: It is respectfully submitted that the FOA text on page 22, lines 9-17, which characterizes the reset RST signal as being "caused by the first bus segment", is not a proper interpretation of Ehata. For example, Ehata paragraph [0007] does not support such teaching. Ehata paragraph [0008] describes the Ehata invention, and shows that there is a "control circuit" of a "device linked to a SCSI bus" which, if active (BSY), "drives a busy (BSY) signal." Driving a BSY signal is an indication of a possible hung situation, and is not an RST, such that no RST is caused by the device #2 in question. According to Fig. 2, "drives" a BSY means that the BSY is connected back to the bus 3 from the device #2 in question, which has that control circuit, and which Fig. 2 shows connected (see line next to "5:BSY") to the bus 3. "Drives" a BSY is not a driving of a RST reset signal 6. Paragraph [0008] further shows that if there is not a BSY on the SCSI bus 3 (see "SCSI bus is not an active state"), that not busy control circuit is "equipped with a means to control to accept the RST on the aforementioned SCSI bus." The "not an active state" means that the device #2 corresponding to that control device #2 is not-hung (not BSY). The "means to control to accept the RST signal" is the later-described circuit 7 of that same device #2, and if not-hung, the RST signal 6 is not accepted by that circuit 7, and no reset of the control circuit of that device #2 occurs. The remarks in paragraph [0056] through [0060] above make it clear that in Ehata, the reset signal received on the first bus segment arrives from the bus 3 and goes to that one device 2.

[0062] The Ehata Purpose Is Not To Isolate The RST Signal From a Second Bus Segment: In paragraph [0056] above, reference was made to the FOA page 23, lines 9-15 rejection, where an assertion was made as to the whole purpose of Ehata. However, that asserted "whole purpose" was not clearly stated, i.e., the following

statement is not clear:

> "...is to allow that having [sic] not hung-up offering [sic] the SCSI control
>
> circuit
>
> which avoids reset processing."

In an attempt to provide a complete response, reference is made to Ehata at page 1, paragraph [0005], where the problem to be solved is stated:

> "...when a hang-up occurs in a certain SCSI device, not only the SCSI device that has hung-up but the SCSI device which has not hung-up is performing reset processing."

The prior art problem was also stated in Ehata paragraph [0006], which refers to that <u>not</u>-hung-up device 2 which <u>has been reset</u> in the prior art, for example:

> "...will be interrupted in the middle of processing...and the SCSI command already published to the SCSI device which has not hung-up was inefficient."

The above remarks in paragraph [0060] make it clear that Ehata <u>does have</u> the purpose asserted by Applicants. That purpose (Ehata page 1, paragraph [0005]) is

> "...the purpose carries out reset processing <u>only</u> of the SCSI device which has hung-up...".
>
> That purpose corresponds to case (b) in paragraph [0060] above, and
>
> that

purpose <u>includes</u> allowing that operating not-hung device to continue to operate independently of the hang-up of the other SCSI device <u>on that same bus segment.</u> Although Ehata achieves that purpose, Ehata does not teach asserting the RST reset

signal on only the first bus segment in a manner by which the first reset signal is normally transmitted through the circuit 7 to a second bus segment, for example, because in both cases (a) and (b) of paragraph]0060] the RST reset signal 6 stops within the device 2.

[0063] Request For Clarification of Interpretation Of Ehata: In view of the numerous times Ehata was cited and discussed in the FOA, it is respectfully requested that, if the next Action continues to assert Ehata, the assertions be consistent, respond favorably to the foregoing discussions in paragraphs [0054] to [0066], not assert any interpretation in which:

(a) more than one bus segment is said to be present in Ehata,

(b) the RST reset signal is said to move through a first bus segment and to a second bus segment, or

(c) Ehata does not teach away from the above limitation of the exemplary claim 9; and

identify with particularity how the circuits 7 of Ehata would be used in combination with House, e.g., where are the circuits 7 located as combined, what is the output of the circuit 7 and where does it go (in terms of the second bus segment).

[0064] The Proper Interpretation of Ehata: Applicants respectfully submit that the remarks in the following paragraphs define a proper interpretation of Ehata, i.e., the interpretation that one skilled in the art would make as to Ehata.

[0065] Proper Interpretation: There Is One And Only One Bus Segment: The Ehata "reset and segment isolation controller" asserted in the FOA at pages 7 and 9 should properly be characterized as one element of one SCSI device of

the many Ehata SCSI devices (shown as three devices identified by "2(#1), 2(#2), and 2(#3)"). It is respectfully submitted that one skilled in the art would recognize that the SCSI bus 3 and those devices 2 make up only one of the claimed bus segments. One SCSI device 2 is connected to a host computer 1 via the one SCSI bus 3 (see Ehata paragraph [0011]). One SCSI bus 3 is coupled in parallel to all of the SCSI devices 2, and to the host computer 1, as shown in Fig. 1. This parallel connection of all of the SCSI devices 2 to the host computer 1 by the bus 3 is referred to above as a "parallel connection" of the devices #2 to the bus 3, and contrasts with the above description of the claimed system as having a "series connection" of the multiple bus segments.

[0066] Proper Interpretation: The RST Reset Signal 6 Is Not Applied From One Device To A Next Device Or Other Bus Segment: One skilled in the art would recognize from the teachings of Ehata noted in paragraph [0060] that none of the Ehata devices 2 receives an RST reset signal 6 from the bus 3 and re-applies that RST signal to the bus 3. In other words, no RST signal is transmitted from device of one bus segment to another device of another bus segment. The RST signal "stops" in each device 2, either before being applied to the circuit 4 (in a not-hung-up device), or upon being applied to the circuit 4 (in a hung-up device 2). Thus, even if one were to consider each device 2 and the bus 3 as one bus segment, there is no teaching of any second bus segment that receives the RST signal from a prior Ehata bus segment. As a result, no RST reset signal 6 applied to the first bus segment can go through that first bus segment to the second (or any next) bus segment.

[0067] Proper Interpretation: The One Bus Segment Interpretation Is Consistent With The Asserted Combination With House: One skilled in the art would recognize that this one bus segment interpretation of Ehata (above paragraph [0059])

is consistent with House, in view of the following. With respect to the main bus 26 shown by House, the Ehata host computer 1 corresponds to one of the computers 14 or 16 which are connected to the main bus 26. Also with respect to the main bus 26 shown by House, the devices 22 of House are directly connected to the main bus 26, which corresponds to the three devices 2 of Ehata that are directly connected in parallel to the SCSI bus 3 (Fig. 1) of the one and only bus segment of Ehata. Also corresponding to the House address ID lines ID-1, etc. for example, Ehata also shows each device 2 as being a last, or end, so-to-speak, device 2 connected to the SCSI bus 3 (resulting from the parallel connection). As described above in paragraph [0061], the RST reset signal 6 on device 2 does not re-applied to the bus 3 (and not thereby applied to another device 2). In other words: (1) one skilled in the art would recognize that the RST that is applied to one device 2 does not connect to any second bus segment in the manner in which the extender 30 of House is connected to the House second bus segment, which is the bus 28+devices 24). That recognition would be based on the fact that in Ehata **no** reset signal 6 is transmitted through any such device 2 of one bus segment to another device 2 of another bus segment, because there is only one bus segment in Ehata. In both House and Ehata, then, the bus and the set of many devices coupled to the bus comprise one claimed "bus segment", which the rejection was careful to note at FOA page 17, lines 13-16.

[0068] Proper Interpretation: Ehata Circuit 7 Is Not An Expander: As so properly interpreted (see above paragraphs [0066] and [0067]), the asserted Ehata "expander" 7 does not enable expansion, or extension, of the one Ehata bus segment (main SCSI bus 3 plus the set of devices 2). Whereas House clearly shows the extender 30 for that purpose, Ehata does not show any corresponding extender connected between the first bus segment (SCSI bus 3 and devices 2) and a further

(second) SCSI bus (see analysis in paragraphs [0056] to [0059] above). Instead, Ehata merely shows the noted one bus segment comprised of the one SCSI bus 3 and all the SCSI devices 2, all such devices being connected in parallel via the SCSI bus 3 of the first, and only, bus segment of Ehata. One skilled in the art would recognize a lack of expander function of the circuit 7 based on the fact that in Ehata the only signal that is applied from any device 2 onto the bus 3 is a BSY signal (see paragraph [0061] above). Further, one skilled in the art would recognize that if the circuit 7 were an expander, then Ehata would teach that other types of signals are output from each device 2 to the bus 3 (in addition to the BSY). In view of these limitations of Ehata, it is respectfully submitted that one skilled in the art would recognize that there is no "expander" in Ehata that would correspond to the extender 30 of House, and would not look to a circuit that is in a device of a bus segment as a basis on which to modify the House expander. Finally, in Ehata there is no element (such as an extender) within which a reset and segment isolation controller could be coupled for the express purpose of isolating a reset signal that is received on the first bus segment of House (bus 26 and devices 22), wherein the isolating would prevent propagation of that reset signal through the extender 30 to the second bus 28 composed of bus 28 and devices 24 (see amended independent claims 9 and 21, for example).

[0069] Proper Interpretation: An Ehata Device Is Not A Bus Segment: In review, the proper interpretation of Ehata does not consider one device 2, as such, as a claimed bus segment. This is consistent with the fact that the rejections do not indicate why one skilled in the art would view any device 2, as such, as a "bus segment" (no less a hung-up device #2 as a first bus segment). See FOA page 9, line 21 in re "first" bus segment; or the reverse, see page 22, line 9, where a not hung-up device #2 is asserted as a first bus segment. It is submitted that to so interpret Ehata

(to have a device 2 of Ehata, as such and without a bus, be a "bus segment", that must have a device and a bus), would be inconsistent with the House teaching (as asserted in the FOA, page 6, lines 13-14) that a first bus segment is bus 26 plus the devices 22, and inconsistent with the FOA at page 17, lines 13-14 (at which the rejection "reminds" the Applicants of the claimed subject matters "bus segment" being limited "to have a set of devices and a bus that is coupled to the set of devices...").

[0070] Proper Interpretation: Ehata Device 2 As Bus Segment Would Be Inconsistent with House: Further, the interpretation of Ehata (to have a hung-up device 2 of Ehata, as such, be a "second bus segment") would be inconsistent with the House teaching of expanding the first bus segment (bus 26 plus devices 22) by means of the expander 30 coupled to the second bus segment comprising auxiliary bus 28 and its devices 24. Having in mind this Ehata lack of an expander (between two such bus segments, as claimed), one skilled in the art would recognize that the Ehata not-hung-up device 2 is not a structure for "expansion" of the first bus segment (bus 3 plus device 2), and also is not a second bus segment. Rather, one would recognize that all of Ehata's devices 2 (whether hung-up or not-hung-up) are and always remain part of the one and only first bus segment of Ehata, and as such are consistent with an exemplary one of House's bus segments comprising devices 22 with the House bus 26.

[0071] Proper Interpretation: Essential Principles of Operation Taught By Ehata: Further, it is respectfully submitted that Ehata teaches essential principles of operation. Those teachings include a teaching that only those Ehata devices 2 that are not hung-up are to be protected from a reset signal that is on the one SCSI bus 3. As applied to House's first bus segment, this teaching is:

Any one of the House not hung-up devices 22 connected to the main bus 26

> is to be protected from a reset signal RST (#6) on the bus 26 by the circuit 7 of Ehata. That circuit 7 is within that not-hung-up device 22. House's bus 26 with RST signal 6 corresponds to Ehata's SCSI bus 3 with RST signal 6, all of which are part of the first bus segment of Ehata. That first bus segment 3 of Ehata includes the SCSI bus 3 and a parallel connection from the bus 3 to each of the SCSI devices 2 shown in Ehata Fig. 1, and thus to each not hung-up device 22 of House's first bus segment.

The asserted uses of the circuit 7 identified in paragraphs [0053] and [0054] appear to propose this use. As applied to House's <u>second bus segment</u>, this teaching would in effect recognize the second bus of House as being comparable to the Ehata <u>first</u> bus segment, and is:

> Any one of the House not hung-up devices 22 connected to the auxiliary bus 28 is to be protected from a reset signal RST (#6) on the bus 28 by the circuit 7 of Ehata. That circuit 7 is within that not-hung-up device 22 on the <u>second</u> bus. House's bus 28 with RST signal 6 corresponds to Ehata's SCSI bus 3 with RST signal 6, all of which are part of a second bus segment similar to the first bus segment of Ehata. That second bus segment 3 of Ehata includes the SCSI bus 3 and a parallel connection from the bus 3 to each of the SCSI devices 2 shown in Ehata Fig. 1, and thus to each not hung-up device 22 of House's first bus segment.

The asserted use of the circuit 7 does not appear to propose this use. For completeness of response, it is noted that in each case of use in the first bus segment or use in the second bus segment, use of the principle of operation would not meet the claim limitations.

[0072] <u>Proper Interpretation: One Asserted Combination Requires Change In Essential Principles of Operation Taught By Ehata:</u> The <u>asserted use</u> of the circuit 7 <u>in the House expander 30</u> would result in blocking the reset signal from <u>all devices</u> on the second bus segment, that is, blocking the RST signal 6 <u>from even the hung-up devices.</u> This is contrary to the purpose of Ehata (see paragraph [0062] above), and would require a change in the design of the circuit 7 of Ehata. The changed circuit 7 would ignore the BSY signal input of a hung device 2, so that <u>any</u>

time the RST signal is applied to the circuit 7 in the expander 30 of House, the RST signal is blocked. That change is illustrated by reference to Ehata paragraph [0023] in which the #1 hung-up device 2 is reset in response to both the BSY of the #1 device and the RST signal 6 driven in connection with that hung-up #1 devices 2. By the asserted changed operation, even though the #1 device 2 still drives the BSY signal, the circuit 4 of that hung-up #1 device 2 on the second bus would not receive the RST signal and would not be reset, contrary to Ehata.

[0073] Proper Interpretation: Ehata/House Combination Does Not Apply Reset Through Expander 30 To Second Bus Segment: Circuit 7 In Device On Bus Segment Does Not Meet Claim Limitations: Paragraphs [0071] and [0072] indicate that in the combination with House, to retain the essential principles of operation of Ehata, the operations of Ehata's circuit 7 should not be inside the expander 30 of House. Rather, the circuit 7 should be located as taught by Ehata in devices 2 on one "side" of the House expander 30 (e.g., on the "side" of the bus 26 or the "side" of the bus 28). Consistent with Ehata, one of the Ehata devices 2 would be connected to the House bus 26 in a manner that would not permit an RST reset signal 6 from one such device 2 to be re-applied to the bus 3. As taught by Ehata, the RST signal 6 "stops" in each device 2, either before being applied to the circuit 4 (in a not-hung-up device) or upon being applied to the circuit 4 (in a hung-up device), and is not re-applied to the bus 3. Thus, even if one were to consider each Ehata device 2 and the bus 3 as one bus segment of House, all of those one bus segments would be part of the House first bus segment, i. e., bus 26 + devices 22, without any series connection of any such bus segment to any other one of such bus segments. As a result, in the proper combination no RST reset signal 6 that is applied to the first bus segment (26 + 22) can go through that first bus segment (22 + 26) to the second (or

any next) bus segment (House 28 + 24) because no circuit 7 would re-apply the reset signal 6, e.g., to the bus 26 of House's first bus segment, or to the bus 28 of House's second bus segment.

[0074] Proper Interpretation: In Asserted Operations, Ehata Teaches Away From Isolating All Signals From Second Bus Segment: In response to the FOA rejection noted in paragraph [0054] above, that rejection asserted that in Ehata the reset RST signal on the first bus segment is isolated from propagating to the second bus segment. However, it was there stated that Ehata describes (1) the first bus segment is not blocked by the reset-condition judging device for receiving the reset RST signal caused by the first bus segment, (2) the second bus segment is blocked by the reset-condition judging device for receiving the RST signal caused by the first bus segment at the same time. It was said that Ehata paragraph [0007] implies that a reset and segment isolation controller isolates a reset signal received on the first bus segment from propagating to the second bus segment. It is respectfully submitted that if the Examiner continues to assert that Ehata has two bus segments and the above operation of (1) and (2) in this paragraph [0074], then the very assertion of operation (1) above shows that Ehata would not isolate all signals. Note that in (1) the rejection states that the first bus segment is NOT blocked, which is understood as meaning that the RST reset signal 6 is transmitted through the first bus segment and to the second bus segment. As described above in paragraph [0060] this is case (a) in which the hung circuit 4 receives the RST signal 6 so as to be reset. Clearly, if any RST signal is not blocked, that not blocked signal is transmitted to the second bus segment, and Ehata does not isolate ALL signals. In this regard, reference is made to the amended claim 9 limitation:

> the first reset and segment isolation controller being further adapted to cause the I/O interface circuits **to isolate all signals** to prevent propagation of the signals between the first and second bus segments during a period after isolating the reset signal until the bus in the first bus segment is cleared from a hang condition.

Accordingly, it is respectfully requested that any next Action acknowledge that Ehata does teach away from the limitation "the reset...controller...adapted...to isolate <u>all</u> signals to prevent..." defined in the exemplary amended claim 9, for example.

[0075] <u>Fourth Discussion: IBM_TBD (herein "IBM"): (cited against claims 1-29)</u>

[0076] <u>Background: FOA Citations:</u> On page 4 of the Final Office Action, in re claims 1-8, IBM was cited as showing one of the claimed features, namely,

> an expander... coupled to a first bus segment ...isolating all communication signals prevents propagation of ... communication signals between first bus ...and other [second] bus...

The asserted teaching of IBM with respect to such isolation of communication signals is the gate 3 coupled between the local bus 13 and the external bus 18.

On page 8 of the FOA, in re claim 9, IBM was cited as showing claimed features, namely,

> an expander controller...isolates **all** signals to prevent propagation of said signals between a first bus segment...and a second bus segment...when a reset signal is asserted...**until** the bus... in said second bus segment is cleared from a hang condition (See the third and fourth paragraphs; i.e., wherein...the diagnostic read enable signal strobes the output of buffer onto the local data bus, and this feature allows the host system to test for invalid states or fault conditions on the external bus **implies** that said expander controller **isolates all** signals **until** the bus in said second bus segment is cleared from a hang condition). (emphasis added)

Similarly, on page 11 as to claims 12 and 24, it was said that IBM

> teaches said expander controller...allows propagation of all signals between said first and second bus segments...when said bus in said second bus segment...is cleared from said hang condition (See the fourth paragraph), which means said second bus is in said BUS FREE state.

On page 10 of the FOA, IBM was cited against claim 21 as showing claimed features, namely,

> an SCSI expander controller ... isolates **all communication** signals to prevent propagation of said communication signals between a first bus segment ...and a second bus segment...when a reset signal is asserted...**until** said second bus is in a BUS FREE state (See the third and fourth paragraphs; i.e., wherein in fact that the diagnostic read enable signal strobes the output of buffer onto the local data bus, and this feature allows the host system to test for invalid states or fault conditions on the external bus **implies** that said expander controller **isolates all** communication signals **until** said second bus is in a BUS FREE state (viz., until the bus in said second bus segment is cleared from a hang condition). (emphasis added)

Also relating to isolation of <u>all</u> signals (i.e., not isolating only communication signals), at FOA page 23, lines 15-16, IBM was asserted as teaching:

> "said expander controller isolates all signals to prevent ..." in lines 15-17 of ...claim 9, which is taught by IBM_TBD (See the instant Office Action, page 8, lines 1-9).

Thus, IBM was cited as showing the claimed (claim 9) isolation of <u>all</u> signals to prevent propagation of the signals between the first and second bus segments, which isolation was claimed as occurring after reset signal isolation and until the bus in the second bus segment is cleared from a hang condition.

On page 11 of the FOA, IBM was cited against claims 11 and 23 as showing claimed features, namely,

> teaches if said bus in said second bus segment...is still hung, said expander controller..., which is said SCSI controller, issues a far-side reset signal...
> to said bus in said second bus segment to reset said second bus segment...
> (claim 11, lines 14-17)

> teaches if said bus in said second bus ...is still hung, said expander controller..., which is said SCSI controller, issues a far-side reset signal...

> to said bus in said second bus segment to reset said second bus segment... (claim 23, lines 18-21)

The far-side reset signal was said to be I/O RESET signal to I/O in the Figure.

On page 12 of the FOA, IBM was cited against claims 14 and 26 as showing claimed features, namely, IBM

> teaches said each expander..., which is said SCSI expander controller, enters into a segment isolation mode...to isolate all signals between said first and second bus segments...

Thus, the segment isolation mode was said to result from the gate 3 being logically disconnected, i.e., gate 3 OFF. Also relating to a segment isolation mode, at FOA page 13, as to claim 20, IBM was cited with House and Ehata, and it was said that the combination suggests

> said reset and segment isolation controller...generates a segment isolation signal (i.e., I/O reset signal from latch 2...), which is provided to all output buffers...to disable output of said communication signals...

Thus, the segment isolation signal was said to be the signal applied to the gate 3 (which signal is the I/O reset signal from latch 2).

[0077] <u>Proper Interpretation of IBM Disclosure:</u> Applicants respectfully submit that a proper interpretation of IBM is set forth in the following paragraphs [ ] through [ ], i.e., the interpretation that one skilled in the art would make as to IBM. IBM describes how computer system expansion may be obtained by connecting an "external unit" to the host system (paragraph 1, lines 1-2). In systems in which that external unit is directly coupled to the host system's I/O bus, faults in the expansion (external) unit may propagate <u>to</u> the host system's I/O bus, making the host system

4-5). IBM provides a "circuit" which logically disconnects the external bus in the external I/O unit from the local bus in the host system (IBM paragraph 1, lines 5-8). Any one of three disclosed events may cause such disconnect. None of those three events relates to clearing the external unit from a hang condition. IBM does not describe any hang condition in of the external unit, but as described below, any such hang condition that may occur would immediately be reset and cleared when an I/O reset is applied to a gate 3 shown in IBM Fig. 1. The gate 3 is turned OFF (controlled) in response to assertion of an I/O reset signal on line 17 by latch 2 (paragraph 1, last few lines). The gate 3 OFF results in

> "isolating external bus 18 from local bus 13" (paragraph 2, line 2).

Specifically, a reset state of latch 2 causes the assertion of the I/O reset on line 17, thus turning the gate 3 OFF. The OFF gate 3 prevents faults in the expansion (external) unit from propagating to the host system, preventing those faults from making the host system inoperative (paragraph 1, lines 4-5).

[0078] Proper Interpretation: Gate 3 Does Not Block Reset Signal: However, the gate 3 does not prevent all signals from passing through the host system's I/O bus to the external bus 18. First, in IBM, there is no host reset signal isolation that would correspond, for example, to the claimed:

> "first reset signal is not propagated through the first expander to the second bus segment..." (amended claim 1), or

> "the first expander controller including a first reset and segment isolation controller coupled between only the first and second I/O interface circuits and adapted to isolate a reset signal received by the expander controller from the first bus segment through the first I/O interface circuit and to the first reset and segment isolator controller so that the reset signal does not propagate through the second I/O interface circuit to the second bus segment,"
>
> (amended claim 9)

In detail, one skilled in the art would consider IBM in its entirety as including the further teaching that no isolation is provided for the I/O reset signal that is asserted on line 17 (see paragraph 2, line 1). That I/O reset signal is asserted on line 17 by latch 2 in response to the output of the OR circuit. Rather than being isolated, this I/O reset signal is applied to both the gate 3 and to the external unit. Contrary to any isolation of the I/O reset signal from that external unit, at IBM paragraph 1, lines 12 and 13, it is expressly stated that

> "The output of latch 2....**provides a reset signal to the external unit**." (emphasis added)

Thus, even though the gate 3 is used to prevent the inbound faults in the expansion unit from propagating to the host system (paragraph 1, line 4), the gate 3 is disclosed as not being effective to prevent the I/O reset signal from being propagated from the host system via the line 17 **outbound** to the external unit (via the I/O). Instead, as the paragraph 1, lines 12-13 quote above shows, the express teaching of IBM is that the output of latch 2 provides the I/O reset signal on line 17 and to the external unit. This external unit corresponds to the claimed second bus segment. Further, one skilled in the art would recognize that the I/O reset signal asserted on line 17 and transmitted to the external unit would reset any hung bus or device that is on the external unit. As a result of the I/O reset signal applied to the external unit, at the **same time** as the gate 3 is turned OFF, there would be a reset of any hung bus or device that is on the external unit. This direct teaching of the I/O reset signal applied to the external unit, plus the well-known result of resetting a bus in response to a reset signal, would be recognized by one skilled in the art as avoiding any need to take any

further steps to reset and clear the external unit. This avoiding of any need to take any further steps to reset and clear the external unit relates to the IBM description of three reset conditions (paragraph 2, line 8) that cause the I/O reset on line 17 to turn on. None of these conditions relates to a hung condition of the external unit. One condition relates to power-on time (paragraph 1, line 9). Another condition is power faults in the external unit (paragraph 2, last line). The last condition relates to software reset condition, in which software issues I/O reset to isolate problems between the local and external buses (paragraph 3, lines 6-7). The cited multiplexer control and diagnostic read are not related by IBM to any hung condition of the external unit (see paragraph 3, lines 7 to end of paragraph). The description at paragraph 4 of IBM in re host system testing for "invalid states" or "fault conditions on the external bus" does not teach or suggest any hung external unit because, by the express teaching of IBM the I/O reset signal is applied by line 17 to the external unit, and because one skilled in the art knows that a reset signal will immediately reset the external unit. As a result, there can only be "invalid states" or "fault conditions on the external bus" other than a hung external unit for the host system to test for via buffer 4, for example. As a result of the description of IBM in this paragraph [0078] **above,** it is respectfully submitted that one skilled in the art would **not** conclude, as the rejections (on FOA pages 8 and 10) concluded, that:

> (See the third and fourth paragraphs; i.e., wherein...the diagnostic read enable signal strobes the output of buffer onto the local data bus, and this feature allows the host system to test for invalid states or fault conditions on the external bus
>
> **implies** that said expander controller **isolates all** signals **until** the bus in ... second bus segment is cleared from a hang condition).

This paragraph [0078] description makes it clear that to reach that conclusion stated in

the rejections, one would have to ignore the (1) direct teaching of the application of the I/O reset signal to the external unit, and (2) result of that application (no hung external unit). It is respectfully submitted that based on the clear direct teachings of IBM, one skilled in the art would not ignore items (1) and (2), but instead would learn from the teachings of IBM and would thus know that no reset or clearing of the external unit would be necessary after the I/O reset signal has been applied to the external unit. Thus, one skilled in the art would know that the IBM disclosure of the diagnostic read enable feature does **not imply**

. that said expander controller isolates all signals until the bus in said second bus segment is cleared from a hang condition.

[0079] Proper Interpretation: Essential Principle Of Operation: I/O Reset Is Applied To External Circuit: IBM teaches an essential principle of operation with respect to the I/O reset signal that is output from latch 2 onto line 17. The principle is to:

> provide the I/O reset signal to the external unit, which reset signal is well-known to reset the bus and devices of the external unit, and
>
> perform that providing of the I/O reset signal at the same time as the I/O reset signal is applied to the gate 3.

This teaching is clear from the above-quoted IBM paragraph 1, last line, for example. Further, as to timing of the I/O reset signal applied on line 17, in IBM there is no teaching as to any delay of the I/O reset signal, neither as to application to gate 3 nor as to application to the external unit. Additionally, in IBM there is no temporal (e.g., "after") relationship between (a) communication signal isolation (via the gate 3) and (b) any asserted "isolation" of the I/O reset signal on line 17. This lack of a temporal relationship is clear first, because there is no isolation of the I/O reset signal that is

asserted on line 17 and that is sent to the I/O and to the external unit to which the host system is extended. Thus, to turn the gate 3 OFF (and as a result to interrupt communication between the external bus 18 and the local bus 13) the reset signal is also simultaneously applied to the I/O reset line 17, and thus to the external unit. As a result, there is no isolation of the I/O reset signal from the external unit to be coordinated (i.e., temporally) with the operation of the gate 3. It is respectfully submitted that in view of this essential principle of operation, if one were to (1) not apply the I/O reset signal to the external unit, or (2) delay the application of the I/O reset signal to the external unit, and thus isolate the I/O reset signal from the external unit for some time period, one would have to change this essential principle of operation. Further, in an endeavor to not change this essential principle of operation one would continue to apply the I/O reset signal to the external unit, and not delay the application of the I/O reset signal to the external unit, and thus not isolate the I/O reset signal from the external unit for any time period. However, to not make the changes would cause the combination to not have the above-noted claim limitations (paragraph [0088] above).

[0080] The Disclosures Of The Combined References:

[0081] Combination 1: Combination 1A is herein defined as the four reference combination as asserted in the FOA against claim 1 (FOA paragraph 3), and as asserted in the FOA against claims 10, 13, etc., (FOA paragraph 5). Combination 1B is herein defined as the three reference combination as asserted in the FOA against independent claims 9 and 21 FOA paragraph 4). It is shown below that these combinations are not proper.

[0082] Combination 1A (Four References), House has a first bus 26 with devices 22; a second bus 28 with devices 24; and an extender 30 between buses

26 and 28. House does not provide reset signals or operation in response to reset signals for clearing bus hang. Instead, House waits for buses to self-clear, by waiting until the main bus becomes free, thus teaching the essential principle of operation that no overt action should be taken to interfere with operation of the hung second bus segment 28 and devices 24. The Looi method relating to the Looi embodiment of Fig. 1 is asserted in the FOA, wherein a first bus segment is expansion bus 61, a second bus segment is expansion bus 62, and the expander is bridge 60. The reset signal (FOA page 3, line 5) is local bus reset signal 68, and the bridge 60 responds to bridge 50. Looi "bus expander bridge 50 of Fig. 1" resets expander bridge 60 in response to a "reset signal". Ehata is combined with its asserted reset and segment isolation controller (in the form of inverter circuit 7 in Fig. 2). Circuit 7 in a device 2 coupled to the House first bus segment (22 + 26) is adapted to isolate the reset RST signal 6 received on the first bus segment and applied to that device 2, which isolation is within the device 2. However, per Ehata the RST reset signal 6 is applied to all elements of the bus segment of Ehata Fig. 1, which means that in combination with House, the RST signal 6 is also applied to the House expander 30, <u>which would not block the RST signal</u>. This relates to not meeting the claim limitations, e.g.:

> in response to the first reset signal asserted on the first bus segment, resetting... and establishing a first reset isolation mode of the first expander to perform reset signal isolation such that the first reset signal is **not propagated** through the **first expander** to the **second** bus segment (amended claim 1);
>
> the first expander controller including a first reset and segment isolation controller coupled between only the first and second I/O interface circuits and adapted to isolate a reset signal received by the expander controller **from the first bus segment through** the first I/O interface circuit and **to** the first reset and segment isolator controller so that the reset signal does **not propagate** through the **second** I/O interface circuit (amended claim 9); and
>
> the SCSI expander controller including a first reset and segment isolation controller coupled between **only** the first and second SCSI I/O interface circuits and adapted to operate in a reset isolation mode to isolate a reset

> **signal received by the SCSI expander controller from the first bus segment through the first SCSI interface circuit** and to the first SCSI interface circuit and to prevent the reset signal from propagating to the second bus segment (amended claim 21)

In this combination of references, the principle of operation of Ehata (that any of the Ehata devices 2 that is not hung-up is to be protected from a reset signal RST (#6) that is on the SCSI bus 3) is used. For the reasons set forth in paragraphs [0071] and [0072] above, Ehata is not interpreted as being added to the House expander 30. In this regard, Paragraphs [0071] and [0072] indicate that in the combination with House, to retain the essential principles of operation of Ehata, the operations of Ehata's circuit 7 should <u>not be inside</u> the expander 30 of House. IBM is asserted in the combination to provide prevention of propagation of communication signals between the first bus 26 of House and the second bus 28 of House. Essential to IBM is also IBM's circuit with gate 3, latch 2, line 17 to I/O which provides the I/O reset signal to the external unit (a second bus segment), and host reset 10. The I/O reset signal to the I/O would reset the second bus segment (external unit) when the gate 3 is turned OFF. Three reset conditions of latch 2 would also be used. Timing of the I/O reset signal on line 17, and to the external circuit, would be the same as timing to turn the gate 3 OFF. The host system tests for invalid states or fault conditions on the external bus implies that said expander controller isolates all communication signals until said second bus is in a BUS FREE state (viz., until the bus in said second bus segment is cleared from a hang condition).

[0083] Combination 1B (Three References): The three references are combined in the same way as in Combination 1A.

[0084] Combination 2: (Proper Four Reference Combination): Combination 2 is herein defined as Applicants' assertion of what the four reference combination would be, as interpreted by one skilled in the art, which would be with:

* House as noted in Combination 1A or 1B (paragraphs [0082] or [0083];

*the disclosure of Looi based on the proper interpretation of Looi advanced above in paragraphs [0046] to [0048], providing the Looi bridge 60 in place of the House extender 60, without control of communication signals and without isolation of the reset signals 54 and 64;

*Ehata's devices 2 applied on the Ehata bus 3 as part of the first bus segment of House, in the manner of House's devices 22 (i.e., Ehata is not inserted into the House extender 30 consistent with above paragraph [0071], and Ehata's RST reset signal 6 is applied to the House expander 30 to propagate to the second bus segment; and

* IBM's expander circuit is added to both the House extender 30 and the Looi bridge 60 for control of communication signals, and as taught by IBM this is without isolation of the IBM I/O reset signal from the second bus segment (external unit), which is consistent with Ehata's reset signal on the first bus segment applied to the House expander 30.

In Combination 2, House includes first bus 26 with devices 22; second bus 28 with devices 24; and the extender 30 between buses 26 and 28. House includes the transceivers 42 and 44 as I/O interface circuits connected to the respective first and

second bus segments 26 and 28, and those transceivers 42 and 44 are connected to an expander controller 46, 48, and 50 between the I/O circuits. House does not provide reset signals or operation in response to reset signals for clearing bus hang (FOA page 3, lines 1-3, page 7, lines 5+, page 9, lines 15+). Instead, House waits for buses to self-clear. To avoid such waiting, consistent with the proper interpretation of Looi (see paragraphs [0046] to [0048] above), the Looi exemplary bridge 60 is used in place of the House extender 30, and is connected to bus 46 (House's bus 26) to receive, and thus respond to, the reset control signal 64. Bus 46 corresponds to a bus of a first bus segment. The bridge 60 (extender) asserts the local bus reset signal 68 on the bus 62 of the second bus segment, which corresponds to House's second bus segment (bus 28 and devices 24). Operation of the extender (Looi bridge 60) is consistent with Looi and is thus in response to the reset control signal 64 applied on the bus 46 of the first bus segment of Looi (or House) to the bridge 60. That bridge 60 operation is to reset the bridge 60, and output the local bus reset signal 68 to bus 62 of the second bus segment. The bridge 60 does <u>not isolate</u> the reset signal 64 from the second bus segment (bus 61, etc.), and instead asserts the reset signal 64 on the bus 61 of the second bus segment as the reset signals 68 and 69. The bridge 60 does not respond to the local bus reset signal 68 that is on the asserted first bus segment 61. The bridge (extender) 60 is not reset in response to the local bus reset signal 68. The bridge (extender) 60 is <u>not</u> caused to isolate the local bus reset signal 68 from the asserted second bus segment, and is consistent with IBM in this regard (as to the reset on line 17 of IBM being sent to the external unit, see paragraphs [0077] and [0078] above). The combination uses Looi's essential principle of operation (above paragraph [0047]), which connects the bridge 60 not only to each of the bus 61 and the bus 62, but also to the further bus 46 so that there can be a response by the bridge

60 to the other reset signal 64). Ehata's devices 2 are applied (as on the Ehata bus 3) to the Looi bus 46 or the House bus 26 as part of the first bus segment of House, in the manner of House's devices 22 (i.e., Ehata is not inserted into the House extender 30 consistent with above paragraph [0071]), and Ehata's RST reset signal 6 is applied to the House expander 30 to propagate to the second bus segment. To provide prevention of propagation of communication signals between the first bus 26 of House and the second bus 28 of House, the combination uses IBM's circuit with gate 3, latch 2, and line 17 to the I/O. Consistent with IBM as noted in paragraphs [0077] and [0078] above, the I/O reset signal is applied to the external unit (a second bus segment) at the time the gate 3 is turned OFF. The I/O reset signal to the I/O resets the second bus segment. The three reset conditions of latch 2 are also used. Consistent with paragraph [0078] above, none of those conditions relates to whether the external unit is or is not hung-up. Further, as there set forth, in IBM there can only be "invalid states" or "fault conditions on the external bus" <u>other than a hung</u> external unit for the host system to test for via buffer 4, and one skilled in the art would not conclude that the IBM diagnostic read enable signal (strobing the output of buffer onto the local data bus and allowing the host system to test for invalid states or fault conditions on the external bus) **implies** that the expander controller isolates all signals until the bus in the second bus segment is cleared from a hang condition.

[0085] <u>Combination 3 (Proper Three Reference Combination)::</u> Combination 3 is Applicants' assertion of what the three reference combination would be, as interpreted by one skilled in the art, which would be with:

* House as noted in Combination 1A or B (paragraphs [0082] or [0083], with transceivers 42 and 44;

* Ehata's devices 2 are applied on the Ehata bus 3 to define a first bus segment, and otherwise as in combination 2;

*that first bus segment of Ehata is consistent with the first bus segment of House, in which the House bus 26 corresponds to Ehata's bus 3, and House's devices 22 correspond to Ehata's device 2; and

*IBM's expander circuit (unnumbered) is used in place of the House extender 30 for control of communication signals, and as taught by IBM this circuit does not isolate the IBM I/O reset signal from the second bus segment (IBM's external unit).

In Combination 3, House includes first bus 26 with devices 22; second bus 28 with devices 24; and extender 30 between buses 26 and 28. House includes the transceivers 42 and 44 as I/O interface circuits connected to the respective first and second bus segments 26 and 28, and those transceivers 42 and 44 are connected to an expander controller 46, 48, and 50 between the I/O circuits. House does not provide reset signals, or a reset and segment isolation controller, or operation in response to reset signals for clearing bus hang. Instead, House waits for buses to self-clear. Consistent with the above paragraph [0073], Ehata's devices 2 are applied on the House bus 26 to define a first bus segment. That first bus segment using Ehata is consistent with the first bus segment of House, in which the House bus 26 corresponds to Ehata's bus 3, and House's devices 22 correspond to Ehata's device 2. Further, consistent with the above paragraph [0068]), Ehata does not have an extender and is thus not inserted into the House extender 30. Also, consistent with the proper interpretation of IBM (see above paragraph [0073], to prevent propagation of communication signals between the first bus 26 of House and the second bus 28 of

House, IBM's circuit with gate 3, latch 2, and line 17 to I/O, provides a reset signal to IBM's external unit (a second bus segment). Consistent with paragraph [0078] above, none of those conditions relates to whether the external unit is or is not hung-up. Further, as stated in paragraph [0078], in IBM there can only be "invalid states" or "fault conditions on the external bus" other than a hung external unit for the host system to test for via buffer 4, and one skilled in the art would not conclude that the IBM diagnostic read enable signal (strobing the output of buffer onto the local data bus and allowing the host system to test for invalid states or fault conditions on the external bus) **implies** that the expander controller isolates all signals until the bus in ... second bus segment is cleared from a hang condition.

[0086] In combination 3, the IBM gate 3 considered as an expander or extender, in combination with the remainder of IBM's "circuit", would not be effective to prevent the IBM I/O reset signal from being propagated from the host system via the IBM line 17 to the external unit (via the I/O). Instead, the express teaching of IBM (see paragraph [0078] above), and the teaching of the essential principle of operation of IBM (see above paragraph [0079]), is that the output of latch 2 provides the reset signal on line 17 and thus to the external unit.

[0087] Referring to paragraph [0079] above, it is clear that an attempt to keep this IBM essential principle of operation with respect to the IBM I/O reset signal that is output from latch 2 onto I/O reset line 17, would require that I/O reset signal be sent to the external unit to allow the system user to power off the external unit (IBM paragraph 3, lines 1-3). It is also clear, however, that there is a **conflict** of (1) keeping this essential principle of operation of IBM (in an endeavor to establish *prima facie* obviousness), and (2) meeting claim limitations, which limitation require that the IBM I/O reset signal on line 17, for example, could not be on the local bus 13 and could not

be controlled by the gate 3. Rather, to not change IBM, the I/O reset signal must be applied around the gate 3, i.e., applied to the I/O and to the external unit notwithstanding the OFF state of that gate 3. The "circuit" of IBM (IBM paragraph 1) is effectively an extender only for the communication signals. This applying of the IBM I/O reset signal "around" (or notwithstanding the OFF of gate 3) is effectively comparable to transmitting the I/O reset signal through the House extender and not having the House extender do any claimed reset signal isolating, because the I/O reset signal on IBM line 17 goes to the IBM external unit, which is IBM's second bus segment (i.e., House's second bus segment 28 + 24). As a result, in IBM combined with House and Ehata in this manner (with Ehata's device 7 in House's devices 22 of the first bus segment, and with IBM's gate 3 in House's extender 30) although there is consistency with Ehata and IBM, there is no claimed isolation of the IBM I/O reset signal from the external unit (House's second bus segment).

[0088] However, the text of amended claim 1, for example, includes:

> in response to the first reset signal asserted on the first bus segment, ...establishing a first reset isolation mode of the first expander to perform reset signal isolation such that the first reset signal **is not propagated through the first expander to the second bus segment**;

Further, the text of amended claim 9 includes:

> including a first reset and segment isolation controller coupled between only the first and second I/O interface circuits and adapted to isolate a reset signal received on the first bus segment by the expander controller from the first bus segment through the first I/O interface circuit and to the first reset and segment isolator controller so that the reset signal **does not propagate through the second I/O interface circuit to the second bus segment,**

Further, the text of amended claim 21 is:

> a first reset and segment isolation controller coupled between **only** the first and second SCSI I/O interface circuits and adapted to operate in a reset isolation mode to isolate a reset signal received by the SCSI expander

controller from the first bus segment **through the first SCSI interface circuit** and to the first SCSI interface circuit and to prevent the reset signal from **propagating to the second bus segment whether or not the second bus segment is in a not hung condition,**

In claim 9, that reset signal is prevented from propagating through the I/O interface circuits, and in all those claims the reset signal does not propagate to the second bus segment.

[0089.] In the cited three reference combination, the situation is thus:

(1) By applying the IBM I/O reset signal on line 17 to the second bus, or by applying Ehata's RST reset signal through the House expander 30, would enable Ehata's teachings of the circuit 7 to be usable in the device 2 of the second bus segment.

(2) Paragraphs [0079] and [0087] note that the use of IBM according to the teachings of IBM (continuing to send reset signal out of the IBM extender to the IBM external unit) is an **attempt to continue** to use the essential principle of operation of IBM, which is necessary to a proper combination that establishes the *prima facie* obviousness.

(3) However, such attempt would not meet:

(a) all claim limitations, which require operations or elements for isolation of the reset signal from the second bus segment, or

(b) the claim 9 text which, for example, requires that reset signal to be prevented from propagating through the expander controller, or

(c) the claim 21 text which, for example, requires preventing the reset signal from propagating to the second bus segment whether or not the second

bus segment is in a not hung condition.

(4) If to meet the claim limitations in re reset signal isolation, IBM were changed to not send the reset signals on the line 17 from the IBM extender to the I/O and thus not to the external unit (second bus segment), the following would also occur. The above essential operating principle of IBM would be **changed** in order to allow the I/O reset signal to be isolated from the second bus segment.

[0090] Applicants Assert That No *Prima Facie* Obviousness Would Result From Combinations 1A, 1B, or 2 Applied To Amended Independent Claims 1, 9, or 21:

[0091] Argument 1: All Of The Combinations With House Are Improper As To All Claims: In the asserted combinations 1A, 1B and 2, House provides a first bus 26 with devices 22; a second bus 28 with devices 24; and an extender 30 between buses 26 and 28. House does not provide reset signals or operation in response to reset signals for clearing bus hang. Instead, House clearly waits for buses to self-clear, in view of the noted House teaching at col. 11, lines 51+.

[0092] It is respectfully submitted that it is not proper to combine any of the other references with House. The above paragraph [0039] makes it clear that the House teaching of waiting until the main bus becomes free, is a teaching of an essential principle of operation. As advanced above in paragraph [0039], that principle is that no overt action (i.e., reset via reset signal) should be taken to interfere with operation of the second bus segment 28 and devices 24. Contrary to this essential principle of operation, the proposed combination would assertedly result in reset of House's second bus segment in response to a reset asserted on the first bus segment and would thus change this essential principle of operation of House. MPEP

2143.01, page 2100-132 makes it clear that if this change is the case, the combined teachings of the art are not sufficient to render the claims *prima facie* obvious. Therefore, it is respectfully submitted that the combination of the three or four references not be further cited against the amended claims.

[0093] As an example of such change of the "wait" operation of House that would result from the asserted combinations, IBM's transmission of the reset signal on line 17 past the gate 3 results in the reset signal being applied to the line 17 and being sent to the I/O and to the external unit (second bus segment). In the manner asserted in the FOA, and when combined with House this IBM I/O reset signal would reset House's expander 30 and second bus segment (bus 28 and device 24), and thus would change that essential principle of operation of House. It is therefore respectfully requested that the combinations based on House not be further asserted against the amended claims.

[0094] Argument 2: The Four Reference Combinations 1A and 2 With Looi Are Improper As To All Claims: The Combinations Would Change An Essential Principle Of Operation of Looi: Without detracting from the validity of the argument in paragraphs [0091] through [0093] above, it is further respectfully requested that Looi not be combined with the other references against the amended claims, for the following reasons:

[0095] Combination 1A As Interpreted In The FOA: The Looi Essential Principle of Operation Would Have To Be Changed: Combination 1A is based on the asserted interpretation of Looi in the FOA (e.g., FOA page 3). There, Looi Fig. 1 was asserted, the first bus segment was said to be 61, the second bus segment was said to be 62, and the bridge 60 was said to couple those first and second

bus segments. The FOA did not assert that the resetting of the bridge (expander) or the isolation of the reset signal on the first bus segment from the second bus segment were in response to the reset signal, and indeed, Looi cannot teach that such resetting or isolation are <u>in response to</u> the local bus reset signal 68 because that local bus reset signal 68 is applied to the bus 61 <u>by the bridge 60</u> (see above paragraph [0043]). Oppositely, as advanced above in paragraph [0047], Looi teaches that it is an essential principle of operation to connect the bridge 60 not only to each of the bus 61 and the bus 62, but also to the further bus 46 so that there can be a response by the bridge 60 to the other reset signal 64. If (as asserted in the FOA, page 18, line 3) there is no connection of the bridge 60 to the bus 48, that essential principle of operation would be changed, specifically would be <u>lost</u>, i.e., the reset control signal 64 would not be received by the expander 60 and the local signals 68 and 69 would not be generated. Again, MPEP 2143.01, page 2100-132 makes it clear that if such change is the case, the combined teachings of the art are not sufficient to render the claims *prima facie* obvious. Therefore, it is respectfully submitted that the combination of the four references not be further cited against the amended claims.

[0096] <u>It Is Not Proper to Use Combination 2: The Looi Essential Principle of Operation Would Have To Be Changed:</u> The discussion in above paragraph [0043] provides sound and adequate reasons as to why one skilled in the art would reasonably interpret Looi so that the bus 46 <u>would be</u> part of the <u>first</u> bus segment of a combination including Looi and House, and why Looi would not be interpreted as asserted in the FOA (with bus 61 part of a first bus segment, bus 62 part of a second bus segment, and no reference to the reset signal 64). This reasoning is consistent with the use of Looi as described in Combination 2. In Combination 2, Looi adds to House the reset control signal 64 applied to the House first bus segment

(main bus 26), and to extender 30 (Looi bridge 60). The Looi bridge 60 (expander), in place of the House extender 30, responds to the signal 64 (col. 4, lines 25+) as taught by Looi. A third bus segment includes the Looi bus segment 62, with appropriate devices, as another output from the Looi bridge 60. The reset control signal 64 causes the bridge (expander) 60 to be reset (col. 4, lines 22-23).

[0097] However, the combined disclosures would further include the teaching of the essential principle of operation of Looi (see above paragraph [0047]) that the bridge 60 responds to signal 64 and outputs the respective local bus reset signals 68 and 69 to the respective second and third bus segments 61 and 62. The combined teaching is that there is no reset isolation or reset isolation mode, and no segment isolation mode. Instead, all devices 24 coupled to each of these second and third bus segments 61 and 62 and are simultaneously reset by the respective local bus reset signal 68 or 69. As advanced above (paragraph [0047]), this output of the two local bus reset signals 68 and 69, one to each of buses 61 and 62, is a teaching that when the reset control signal 64 is applied to the bridge 60, the bridge (expander) 60 should not isolate the original reset control signal 64 from either of the second or the third buses 61 and 62. This teaching means that even though the buses and the devices of the second and third buses 61 and 62 are not hung, those buses and the devices of those buses 61 and 62 will be reset, and will be reset in response to the reset control signal 64 without regard to whether or not the device is hung-up or not hung-up.

[0098] It is respectfully requested that Combination 2 (with Looi) not be cited against the amended claims. First, as advanced above in paragraph [0047], this action of outputting local bus reset signals 68 and 69 is a teaching of an essential principle of operation of Looi. Second, to meet every limitation of the claims this

principle would have to be changed. For example, one would have to change the essential principle of operation of Looi to meet clause b) of independent claim 1 (and dependent claims thereon), e.g., to obtain in Looi the claimed isolation of the reset signal from the second bus segment) because Looi transmits the reset signals 68 and 69 in response to the reset signal 64, effectively transmitting the reset signal 64 past the bridge 60, for example. That change would be to stop (and thus isolate) the local signals 68 and 69 from each of two bus segments of which buses 61 and 62 are a part. Further, to meet clause c3) of amended claim 1, a reset isolation mode would have to be established, and based on the recited condition a far-side reset signal would have to be applied to the second bus segment. Also, the changes would have to be made to provide the limitations of independent claims 9 and 21. Again, MPEP 2143.01, page 2100-132 makes it clear that if such change is the case, the combined teachings of the references are not sufficient to render the claims *prima facie* obvious. Therefore, it is respectfully submitted that Combination 2 of the four references not be cited against the amended claims.

[0099] Argument 3: The Four Reference Combination 2 With Looi Is Improper As To All Claims: The Combination Does Not Include All Claim Limitations: As a further reason based on the combinations with Looi, it is respectfully requested that the combination with Looi not be cited against the amended claims. For completeness of response, although there is no reason other than Applicants' claims to do so, an attempt could be made to avoid the above-noted changes to the Looi essential principle of operation. This attempt would continue to respond to the reset signal 64 by continuing to apply signals 68 and 69 simultaneously to the respective second or the third bus segments 61 or 62. However, that attempt

would not meet the claim text which requires operations or elements for isolation of the reset signal from the second bus segment. The buses 61 and 62 are parts of the respective second and third bus segments, and the continued application of one or both of those signals 68 and 69 to the respective second and third bus segments would be the opposite of the claimed isolation. Further, with these operations of Looi performed to transmit the reset signal 68 and 69 to the second bus segments without any delay, operation c2) of amended claim 1 would not be met, and the conditional operation of claim 1 clause c3) would not be met. Also, the expander controller limitations of amended claims 9 and 21 would not be met. Again, when the combination fails to meet every claim limitation, MPEP 2143.03, page 2100-133 is applicable, and provides that *prima facie* obviousness is not established. Therefore, it is respectfully submitted that the combination of the four references not be cited against the amended claims because such combination based on use of this essential principle of operation of Looi would not teach or suggest all claim limitations.

[0100] Argument 4: All Combinations With Ehata Are Improper As To All Claims: None of The Combinations Includes All Claim Limitations: For a further reason, that is based on Ehata, it is respectfully requested that none of the asserted combinations of references be cited against the amended claims.

[0101] Combinations 1A and 1B: Ehata Used In First Bus Segment: Use of the Ehata essential principle of operation in these three and four reference combinations would not meet the claim text which requires operations or elements for isolation of the reset signal from the second bus segment. Contrary to the assertion in the FOA (page 7, line 9, for example) it is made clear in paragraph [0068] above that in Ehata there is no element (such as an expander) within which a reset and segment isolation controller could be coupled for the claimed purpose of isolating a reset

signal that is received on the first bus segment of House (bus 26 and devices 22), wherein the isolating would prevent propagation of the reset signal through the expander (or through an expander controller) 30 to the second bus 28 composed of bus 28 and devices 24 (see amended independent claims 9 and 21). Rather, the recognition of, and retained use of, that principle of operation of Ehata (paragraph [0071]) in the combined references would only result in one or more of the House devices 22 connected to the main bus 26 (of the first bus segment) being protected from a reset signal RST (#6) on the first bus segment (bus 26). The protection would be by the circuit 7 of Ehata in the device 22 of House that is not hung-up. No claimed protection of any second bus segment (e.g., of House) would be obtained because Ehata's protection of the devices 2 from the RST reset signal 6 via that essential principle of operation only applies to the devices 2 on the first bus segment (including bus 3). Moreover, per Ehata the RST signal 6 would be applied to the expander 30 of House, and no isolation would occur. Further, paragraph [0072] above makes it clear that the circuit 7 should not be inserted into the expander 30 of House. Thus, another claim limitation is not present in the combined references. MPEP 2143.03, page 2100-133 makes it clear that if all claim limitations are not met, the combined teachings of the references are not sufficient to render the claims *prima facie* obvious. Therefore, it is respectfully submitted that the combination of the four references not be cited against the amended claims.

[0102] Ehata Used In Second Bus Segment In Four Reference

Combination: Even if an attempt were made to use Ehata's principle of operation in the second bus segment of House (i.e., applied to one or more devices 24 of the auxiliary bus 28), no claimed isolation of that second bus segment of House would be

obtained. This lack of isolation results from Ehata's isolation of devices 2 of the second bus segment being effective only if the RST reset signal 6 is applied through the expander of House (or Looi) to the second bus segment, and by the second bus to that very device 2 on the second bus. In this combination with House and Looi, in response to the reset signal 64 asserted on the bus 46 of the first bus segment of Looi, there would be resetting of the first expander 60 coupled to the first bus segment. However, as is made clear above (paragraph [0047]), to keep the essential operating principle of Looi, the Looi local bus reset signal 68, for example, must be applied to the bus 61 of the second bus segment (of House's bus 28 + devices 24). As a result, in House and Looi combined with Ehata, to be consistent with Ehata, the local bus reset signal 68 would be applied through the extender 30 of House (contrary to House using no reset signals) and would be applied to the second bus of House (bus 28) so as to be applied to one of the devices 24 of House (consistently with Ehata sending the RST signal 6 to a device 2). For the operation of the Ehata circuit 7, Ehata would thus rely on the exemplary Looi reset signal 68 being applied through the Looi bridge 60 (or through the House extender 30), for example, on the second bus (including a device 2 of Ehata). Only then would Ehata's teachings be usable in the device 2 (House 24) of the second bus segment. However, paragraph [0088] notes claim limitations not present in the combination. The situation is thus:

(1) Only by applying the reset signal 68 onto the second bus would Ehata's teachings of the circuit 7 be usable in the device 2 of the second bus segment.

(2) Paragraph [0047] notes that the use of Looi according to the teachings of Looi (continue to send signal 68 out of Looi's bridge 60) is an attempt to continue to respond to the reset signal 64 by continuing to apply the signal 68

to the respective second bus segment 61, and is an attempt to keep the essential principles of operation of Looi.

(3) However, such attempt would not meet all claim text identified in paragraph [0088], which for example requires operations or elements for isolation of the reset signal from the second bus segment, and would not meet claim 9 text by which that reset signal is prevented from propagating through the expander controller to the second bus segment,.

(4) If Looi were changed to not send the signals 68 or 69 from the bridge 60, Ehata would not have a RST reset signal 6 to apply to the circuit 7 in the second bus segment. Thus to have Ehata be usable, Looi's teachings (essential principles of operation) of the signals 68/69 being applied through the expander bridge 60 would have to be followed.

(5) Paragraph [0043] would apply to Ehata combined with House and Looi, such that the arguments made there would apply. Thus, the buses 61 and 62 are parts of the respective second and third bus segments, and the continued application of one or both of those signals 68 and 69 would not provide these isolation claim limitations.

(6) As a result of the application of the signals 68/69 on the second bus segment, this operation of the combined House and Ehata references will not result in resetting one bus segment at a time (as defined in claims 8, 18, and 29).

When the combination fails to meet every claim limitation, MPEP 2143.03, page 2100-133 is applicable, and provides that *prima facie* obviousness is not established.

Thus, even if Ehata were to be asserted as being usable in the second bus segment of House with Looi, the reset signal which Ehata would require in the second bus segment would cause the combined references to fail to meet every claim limitation, and would be a combination that does not establish *prima facie* obviousness.

[0103] Ehata Used In Second Bus Segment In Three Reference Combination: Even if an attempt were made to use Ehata's principle of operation in the second bus segment of House (i.e., applied to one or more devices 24 of the auxiliary bus 28), no claimed isolation of that second bus segment of House would be obtained in the three reference combination. Again, this lack of isolation results from Ehata's isolation of devices 2 of the second bus segment being effective only if the RST reset signal 6 is applied through the expander of House (or through the "circuit" of IBM "which logically disconnects...", page 1, paragraph 1) to the second bus segment, and by the second bus to that very device 2 on the second bus. In this three-way combination with IBM, , there is no host reset signal isolation because IBM teaches that such circuit does not do the claimed isolation of the host reset signal 10. Rather, in this "circuit" of IBM, this host reset signal 10 is applied through an OR circuit to latch 2, and the latch 2 (that turns gate 3 OFF) does not also isolate the reset signal 10 from the I/O that is connected to the external unit. Contrary to such isolation of the reset signal from that external unit, as described above in paragraph [0078] above, IBM at paragraph 1, lines 12 and 13 clearly teaches that "The output of latch 2....provides a reset signal to the external unit."

[0104] Thus, even if the Ehata circuit 7 is considered as an expander, or extender, that circuit 7, in combination with IBM's "circuit", would not be effective to prevent the IBM reset signal from being propagated from the host system

via the IBM line 17 to the external unit (via the I/O). Instead, as quoted above, the express teaching of IBM, and the teaching of the essential principle of operation of IBM, is that the output of latch 2 provides the reset signal on line 17 and to the external unit. Reference is made to paragraph [0079] above. There it is made clear that under this essential principle of operation with respect to the reset signal that is output from latch 2 onto I/O reset line 17, the reset signal is sent to the external unit to allow the system user to power off the external unit (paragraph 3, lines 1-3). It is also clear, however, that to keep this essential operating principle of IBM (in an endeavor to establish *prima facie* obviousness) the IBM reset signal on line 17, for example, must be applied around the gate 3, or applied to the I/O and the external unit notwithstanding the OFF state of that gate 3. The "circuit" of IBM (paragraph 1) is effectively an extender only for the communication signals. This applying of the IBM reset signal "around" (or notwithstanding the OFF of gate 3) is effectively comparable to being through the House extender, because the reset signal on IBM line 17 goes to the IBM external unit, which is IBM's second bus segment (i.e., House's second bus segment 28 + 24). As a result, in IBM combined with House and Ehata, and consistent with Ehata and IBM, the reset signal would be applied through the extender 30 of House (contrary to House using no reset signals) and would be applied to the second bus 28 of House's second bus segment (bus 28 + devices 24) so as to be applied to one of the devices 24 of House as taught by Ehata's application of RST signal 6 to device 2.

[0105] Further, for the operation of the Ehata circuit 7, Ehata would thus rely on the IBM reset signal being applied on line 17 effectively through the IBM extender (or the House extender 30), onto the second bus (IBM's external unit). Only then would Ehata's teachings be usable in the device 2 of the second bus segment,

i.e., in the device 24 of House. However, as set forth in paragraph [0088], this does not meet the text of amended claims 1, 9, and 21, for example. The situation is thus:

(1) Only by applying the IBM reset signal on line 17 to the second bus would Ehata's teachings of the circuit 7 be usable in the device 2 of the second bus segment.

(2) Paragraph [0078] notes that the use of IBM according to the teachings of IBM (continuing to send reset signal out of the IBM extender to the IBM external unit) is an attempt to continue to use the essential principles of operation of IBM, which is necessary to a proper combination that establishes the *prima facie* obviousness.

(3) However, such attempt would not meet all claim text which requires operations or elements for isolation of the reset signal from the second bus segment, and would not meet the claim 9 text by which that reset signal is prevented from propagating through the expander controller.

(4) If to meet the claim limitation in re reset signal isolation, IBM were changed to not send the reset signals on the line 17 from the IBM extender to the I/O and thus not to the external unit (second bus segment), two events would also occur. First, the above essential operating principle of IBM would be changed. Second, the claim limitation of reset signal isolation would not result because Ehata would not have a RST reset signal 6 to apply to the circuit 7 for isolation purposes.

For these further reasons in Argument 4, it is respectfully submitted that the asserted combinations of references not be cited against the amended claims.

[0106] Argument 5: The Combination With Ehata Is Improper As To All Claims: The Combination Does Not Include All Claim Limitations: For a further reason based on Ehata, it is respectfully submitted that the combination of the four references not be cited against amended claims 1-29. It is submitted that the Ehata operation, which is described as a "mask of the RST signal 6" in paragraph [0024], would not be recognized by one skilled in the art as being related to or enhancing any operation of the extender 30 of House for the following reasons:

(1) Ehata only shows the one SCSI bus 3 (corresponding to House's main bus 26), and this one bus 3 is part of the above-noted first bus segment that also includes all of Ehata's devices 2.

(2) Ehata's purpose is described only with respect to the devices 2 that are on that one bus 3, i.e., that are on the first bus segment. As noted above, Ehata describes its purpose in terms of a problem (see paragraph [0005]) in which the reset signal 6 intended to reset one such (hung-up) device 2 of the first bus segment also resets a not-hung-up device 2 that is on the same first bus segment (that includes bus 3).

(3) This purpose of Ehata is not related to the expanding function of the House expander 30, because Ehata properly teaches only use of the masking circuits 7 in each of the devices 2 that are on the first bus segment (see paragraph [0067] above). These devices 2 would be coupled to the Ehata bus 3 before any expander 30 of House, and do not, and would not, rely on the operation of any such expander 30 for their intended operation.

(4) Even if one skilled in the art were to accept the masking circuit 7 of each device 2 of Ehata as being fully applicable to a combination with House, Ehata

would reasonably teach one skilled in the art to put one such circuit 7 only in each first bus segment device 22 of House. It is respectfully submitted that this limitation to the first bus segment is proper because there is no basis in Ehata or House by which one skilled in the art would be motivated to modify House by placing any circuit 7 of Ehata in the expander of House. This lack of such motivation is clear from the fact that the purpose of Ehata would be achieved in combination with House by following Ehata's teachings, which would instruct to put one such circuit 7 in each first bus segment device 22 of House. This Ehata purpose would be achieved both in terms of not resetting a not-hung-up device (due to isolating the RST reset signal 6 from that not-hung-up device 2, see Ehata paragraph [0024]), and in terms of resetting only a hung-up device 2 (Ehata paragraph [0023]), and without changing the essential operating principle of Ehata (paragraph [0071] above).

(5) Moreover, this lack of such motivation is clear from the fact that in each of Ehata's paragraphs [0023] and [0024] applied to a device 2 on the first bus segment per case (4), the RST signal 6 of Ehata would not be applied to any second bus segment of House if the teachings of Ehata were followed. Case (4) would thus avoid changing (isolating) any reset signal (e.g., Looi or IBM) normally output to the second bus segment (the essential principle of operation of Looi and IBM).

(6) However, in terms of whether the thus interpreted combination would establish *prima facie* obviousness, by definition case (4) does not provide an isolation of a reset signal that is on the first bus segment, where the isolation prevents propagation of the reset signal to the second bus segment, as claimed.

Moreover, the above asserted "selective" reset of a device (per case (4) is not a claimed "selective" reset of a device that is on the second bus segment. Thus, Ehata in combination with the three other references (re claims 1-8) or Ehata in combination with the other two references (claims 9-29) would not establish *prima facie* obviousness because the combination would not have all of the claim limitations.

For these further reasons in Argument 5, it is respectfully submitted that the asserted combinations of references not be cited against the amended claims.

[0107] Argument 6: The Combinations With IBM Are Improper As To All Claims: The Combinations Do Not Include All Claim Limitations: IBM was cited (page 4) for a limited purpose, namely isolating the communication signals, assertedly relating to operations c) in claim 1, for example. It is respectfully submitted that the purpose for which IBM was cited would be no justification for ignoring the assertion in paragraph [0078] above that IBM sending the reset signals from the line 17 to the second (external unit) bus segment is an essential operating principle of IBM, and thus one that is not to be changed if prima facie obviousness is to be established. Further, in view of the remarks above in re the deficiencies of Ehata as to isolation of the reset signal, one skilled in the art would be more likely to consider IBM in combining an extender with a second bus segment. However, reference is made to the remarks in paragraph [0078] re IBM teaching an essential principle of operation with respect to the reset signal that is output from latch 2 onto I/O reset line 17, and in re providing the reset signal to the external unit, which allows the system user to power off the external unit (paragraph 3, lines 1-3), for example. Those remarks clearly indicate that for purposes of establishing prima facie

obviousness it is not proper to ignore or change this essential principle of operation. Further, if that essential principle of operation is not changed, the combination with IBM does not include all claimed limitations. In either event, the combinations with IBM are improper as to all claims. Further, as a result of the description of IBM in paragraph [0078] above, it is respectfully submitted that one skilled in the art would **not** conclude, as the rejections (on FOA pages 8 and 10) concluded, that:

> (See the third and fourth paragraphs; i.e., wherein...the diagnostic read enable signal strobes the output of buffer onto the local data bus, and this feature allows the host system to test for invalid states or fault conditions on the external bus
>
> **implies** that said expander controller **isolates all** signals **until** the bus in ... second bus segment is cleared from a hang condition).

The paragraph [0078] description makes it clear that to reach that conclusion stated in the rejections, one would have to ignore the (1) direct teaching of the application of the I/O reset signal to the external unit, and (2) result of that application (no hung external unit). It is respectfully submitted that based on the clear direct teachings of IBM, one skilled in the art would not ignore items (1) and (2), but instead would learn from the teachings of IBM and would thus know that no reset or clearing of the external unit would be necessary after the I/O reset signal has been applied to the external unit. Thus, one skilled in the art would know that the IBM disclosure of the diagnostic read enable feature does **not imply** that said expander controller isolates all signals until the bus in said second bus segment is cleared from a hang condition. Thus, a claim limitation resulting from the attempt to imply would not be obtained. For these further reasons in Argument 6, it is respectfully submitted that the asserted combinations of references with IBM not be cited against the amended claims.

In view of these remarks and the amendments to the claims, allowance of the claims is respectfully requested.

Respectfully submitted,

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